


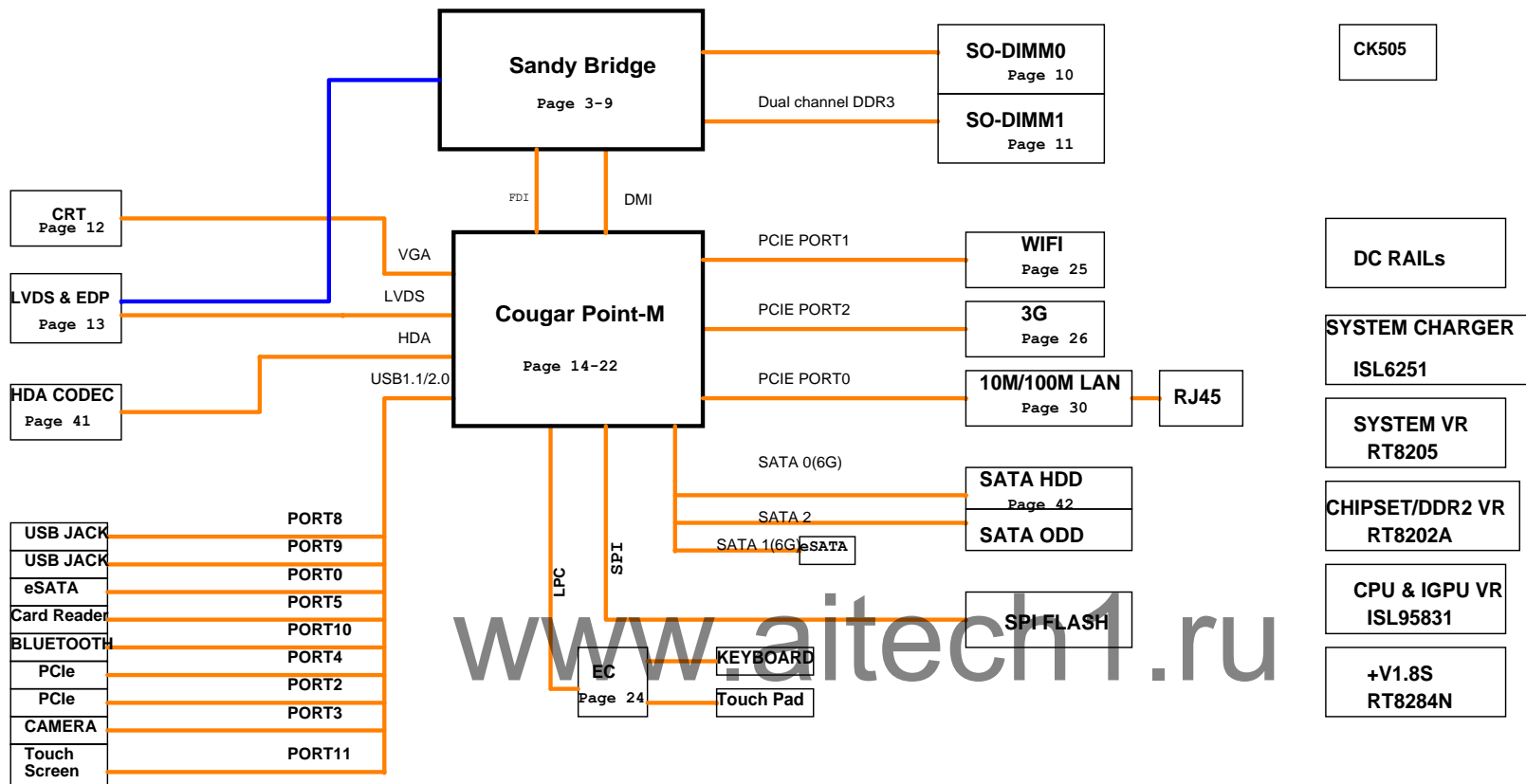
**E450**


# Sandy Bridge Mobile PROCESSOR With Cougar Point-M

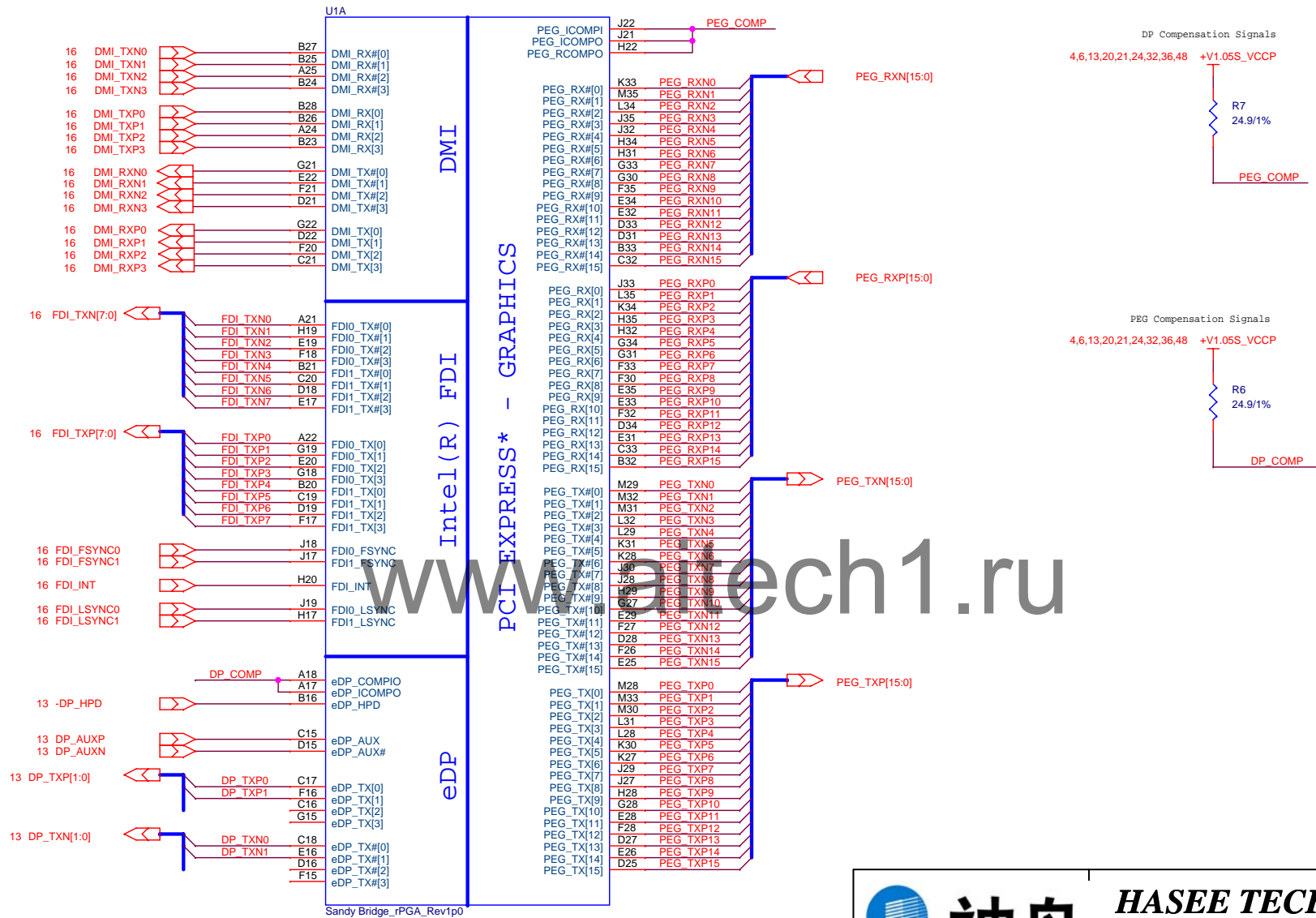
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June 2010  
Revision 0.2

 <b>神舟</b> HASEE		<b><i>HASEE TECHNOLOGY INC.,</i></b>		
		<b>Cover Page</b>		
Draw by LIZX	Size B	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model <b>E450</b>	Sheet 1	of 50



 <b>神舟</b>		<b>HASEE TECHNOLOGY INC.,</b>	
<b>Block Diagram</b>			
Draw by Thursday, May 22, 2014	Size B	CAGE Code <Cage Code>	DWG NO Rev 0.2
Scale	Model <b>E450</b>	Sheet 2 of 50	





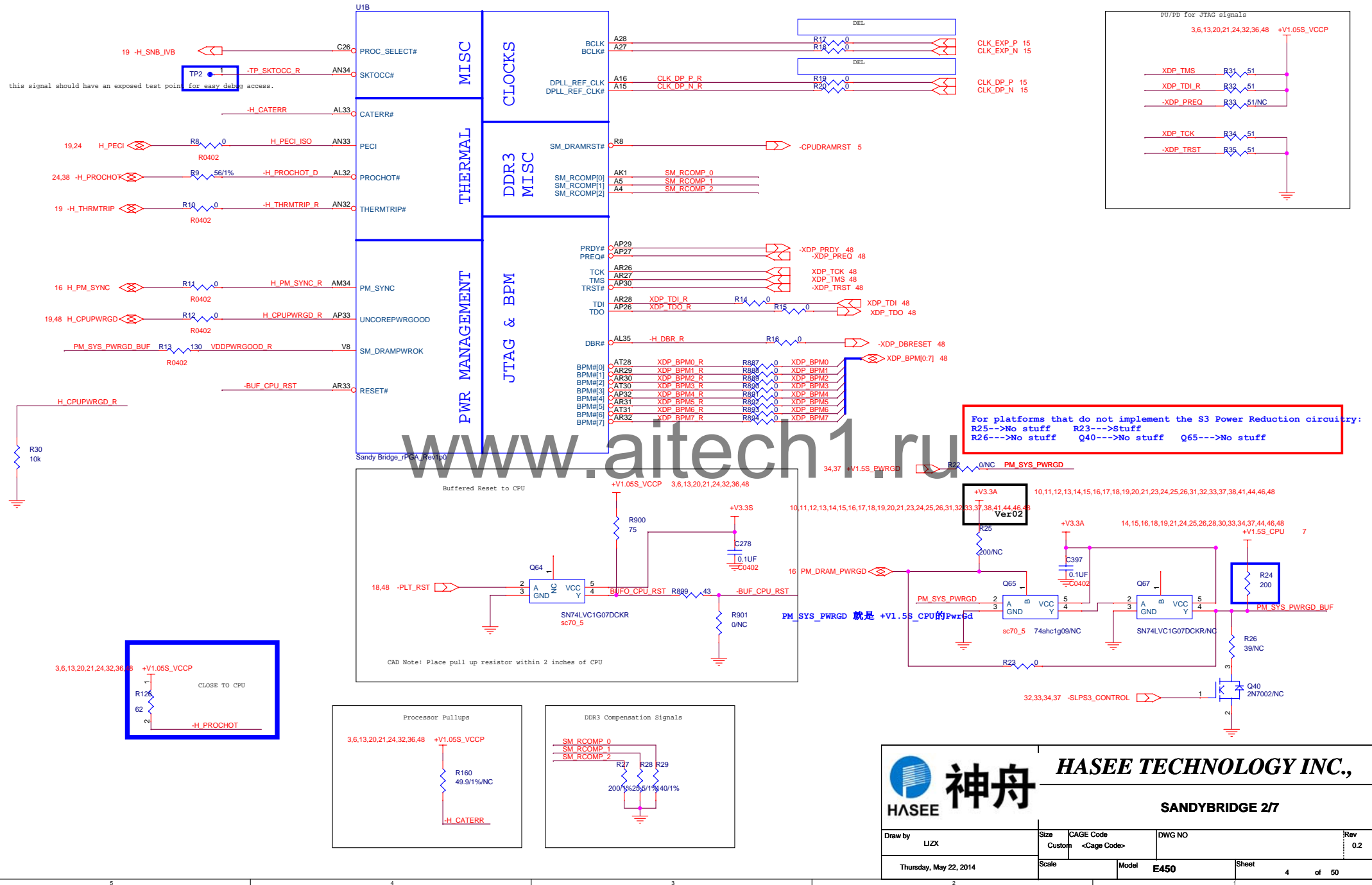
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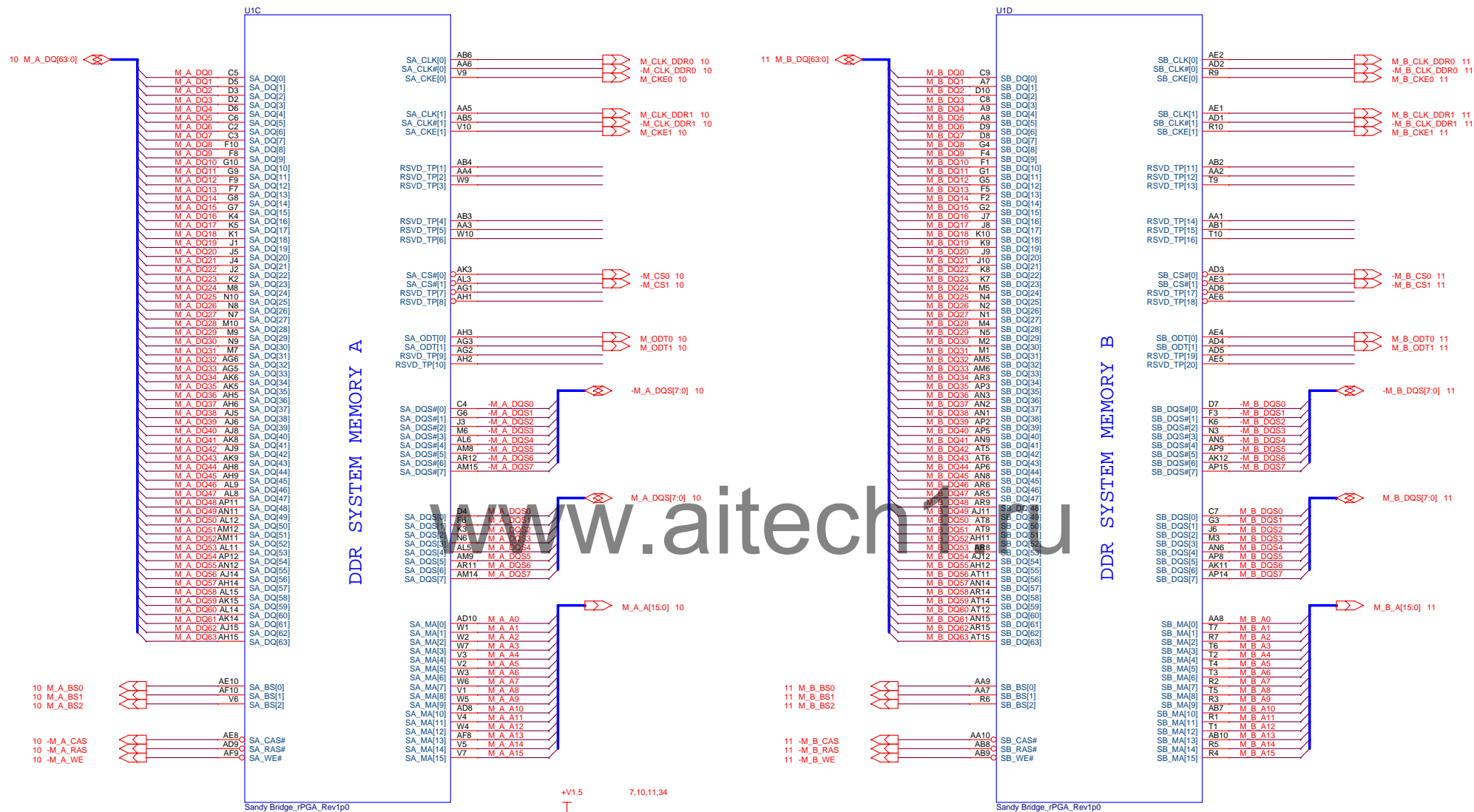
HASEE

## HASEE TECHNOLOGY INC.,

### SANDYBRIDGE 1/7

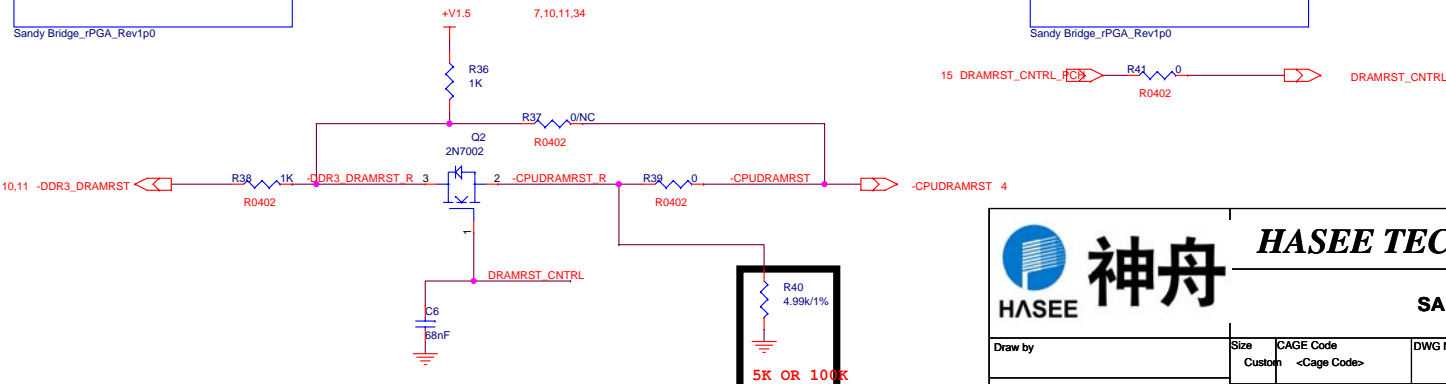
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Thursday, May 22, 2014	Scale	Model <b>E450</b>	Sheet 3 of 50	





Sandy Bridge\_rPGA\_Rev1p0

Sandy Bridge\_rPGA\_Rev1p0



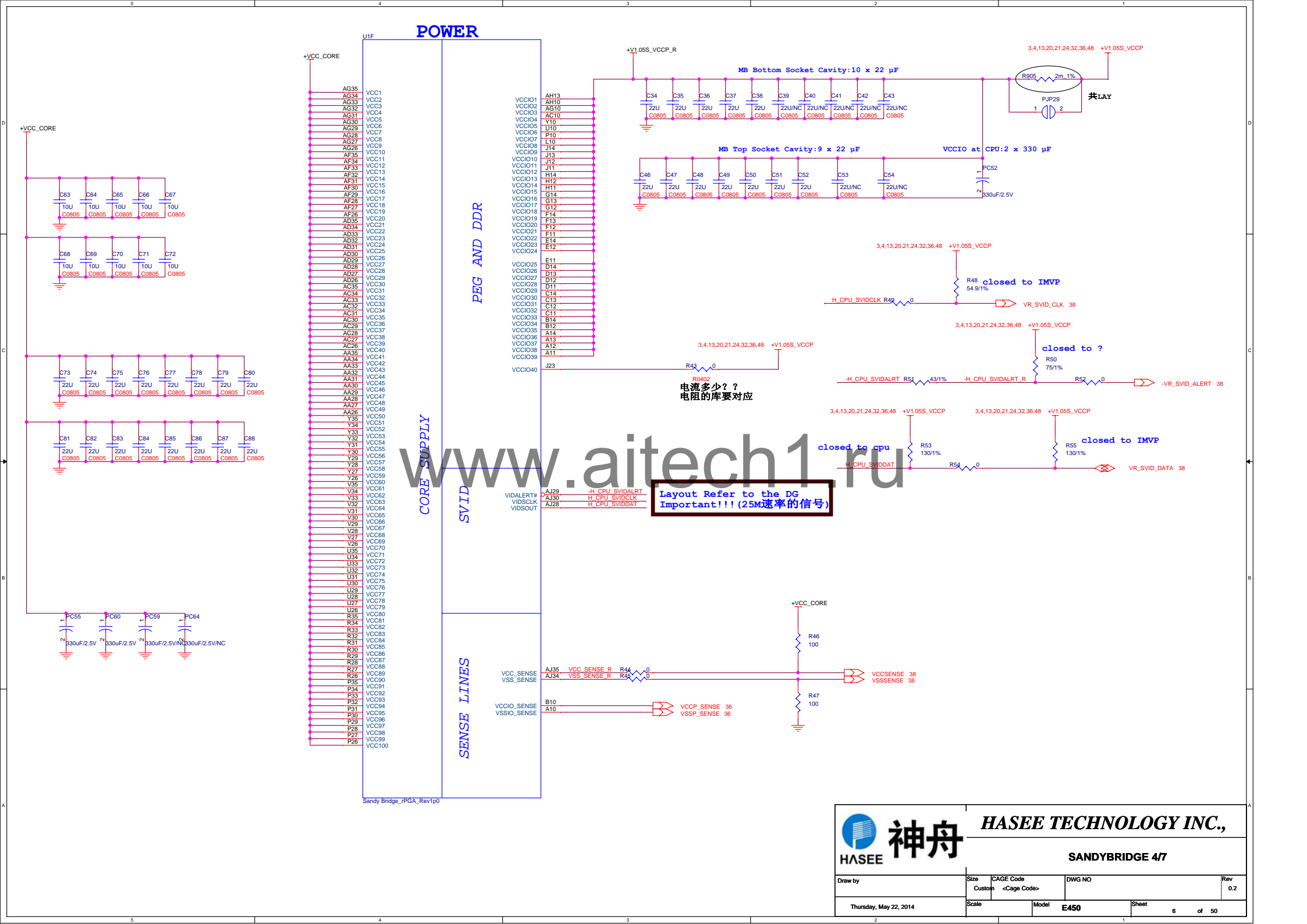
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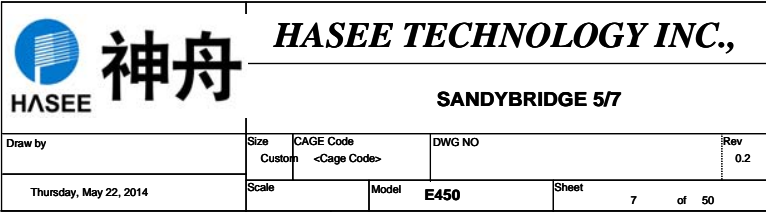
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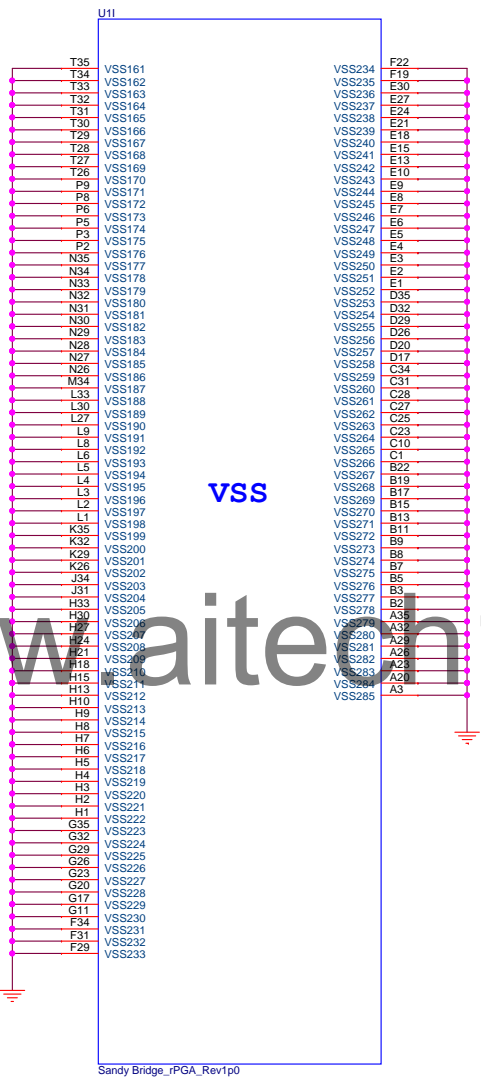
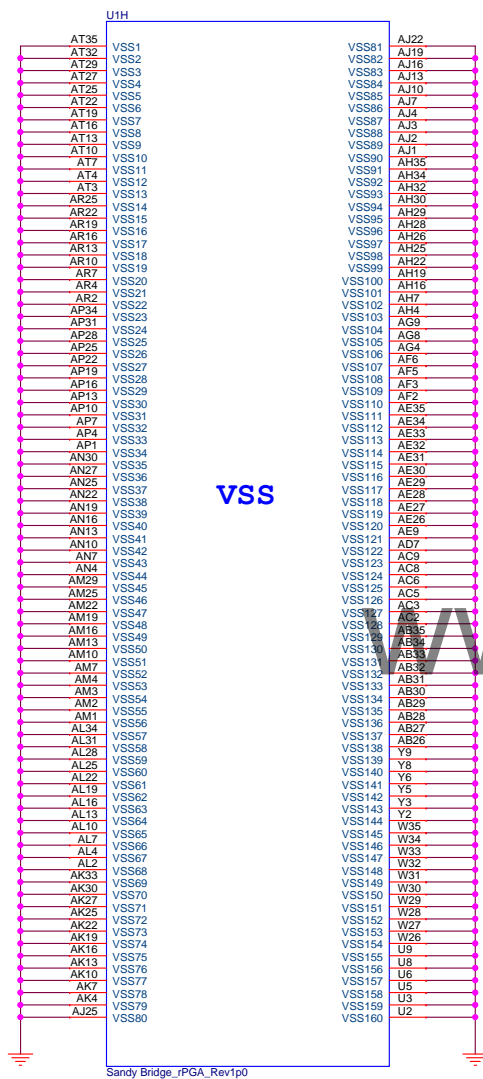
## HASEE TECHNOLOGY INC.,


### SANDYBRIDGE 3/7

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	Custom	<Cage Code>		0.2
Thursday, May 22, 2014	Scale	Model	E450	Sheet 5 of 50







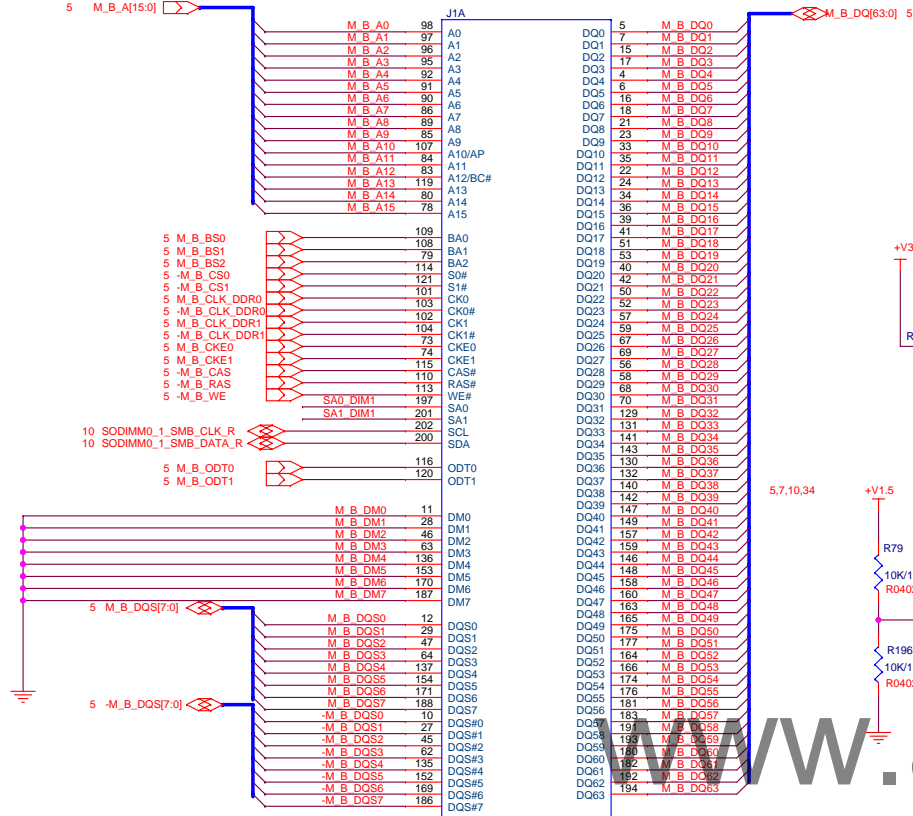
 <b>HASEE 神舟</b>		<b>HASEE TECHNOLOGY INC.,</b> <b>SANDYBRIDGE 6/7</b>		
Draw by	Size	CAGE Code	DWG NO	Rev
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Thursday, May 22, 2014	Scale	Model	E450	Sheet 8 of 50



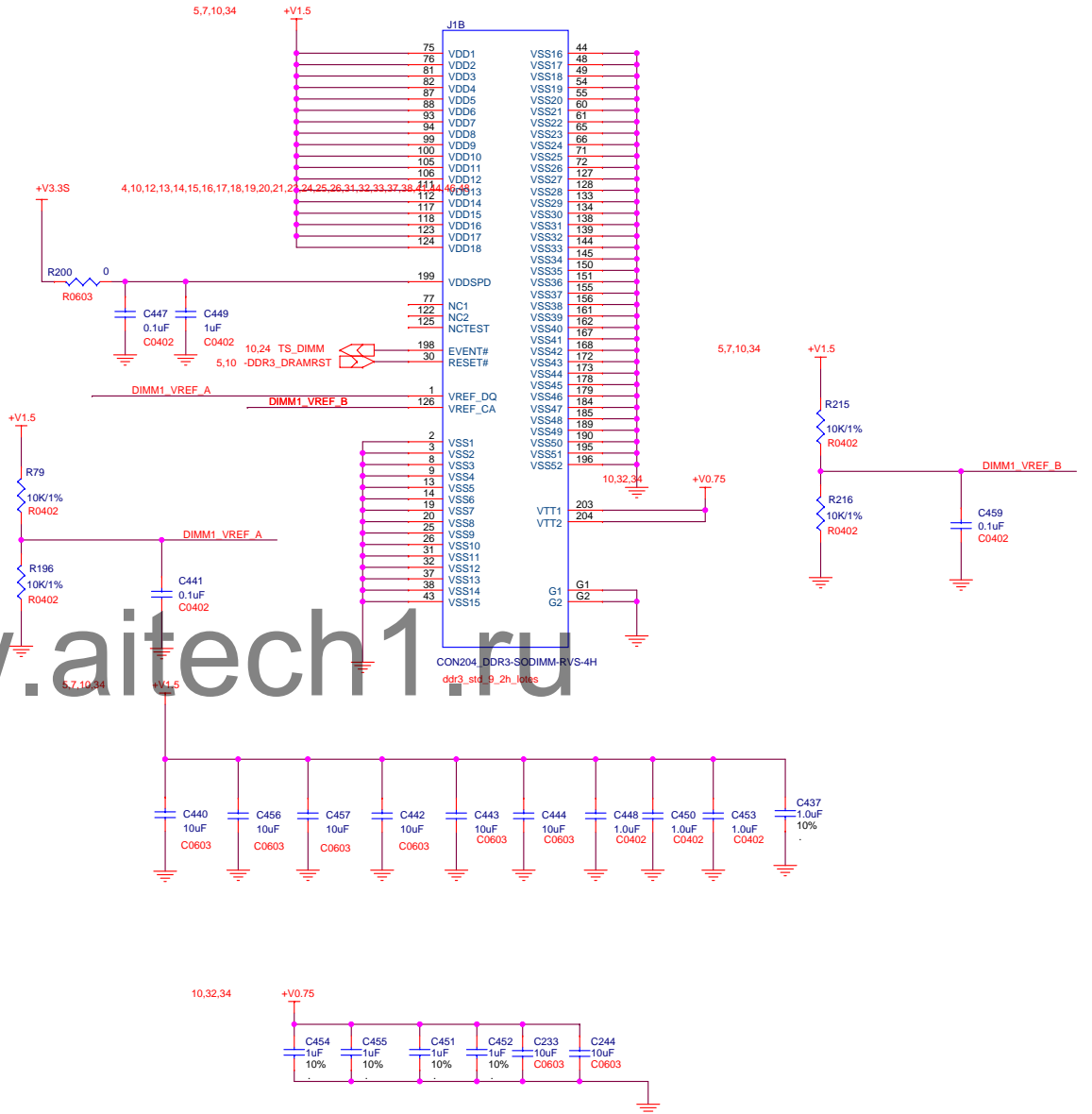
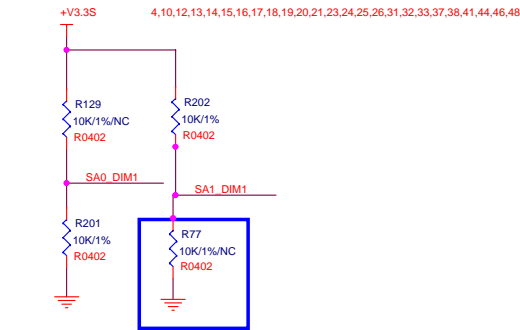





# SODIMM-B H9.2



CON204\_DDR3-SODIMM-RVS-4H  
ddr3\_std\_9\_2h\_totes





神舟

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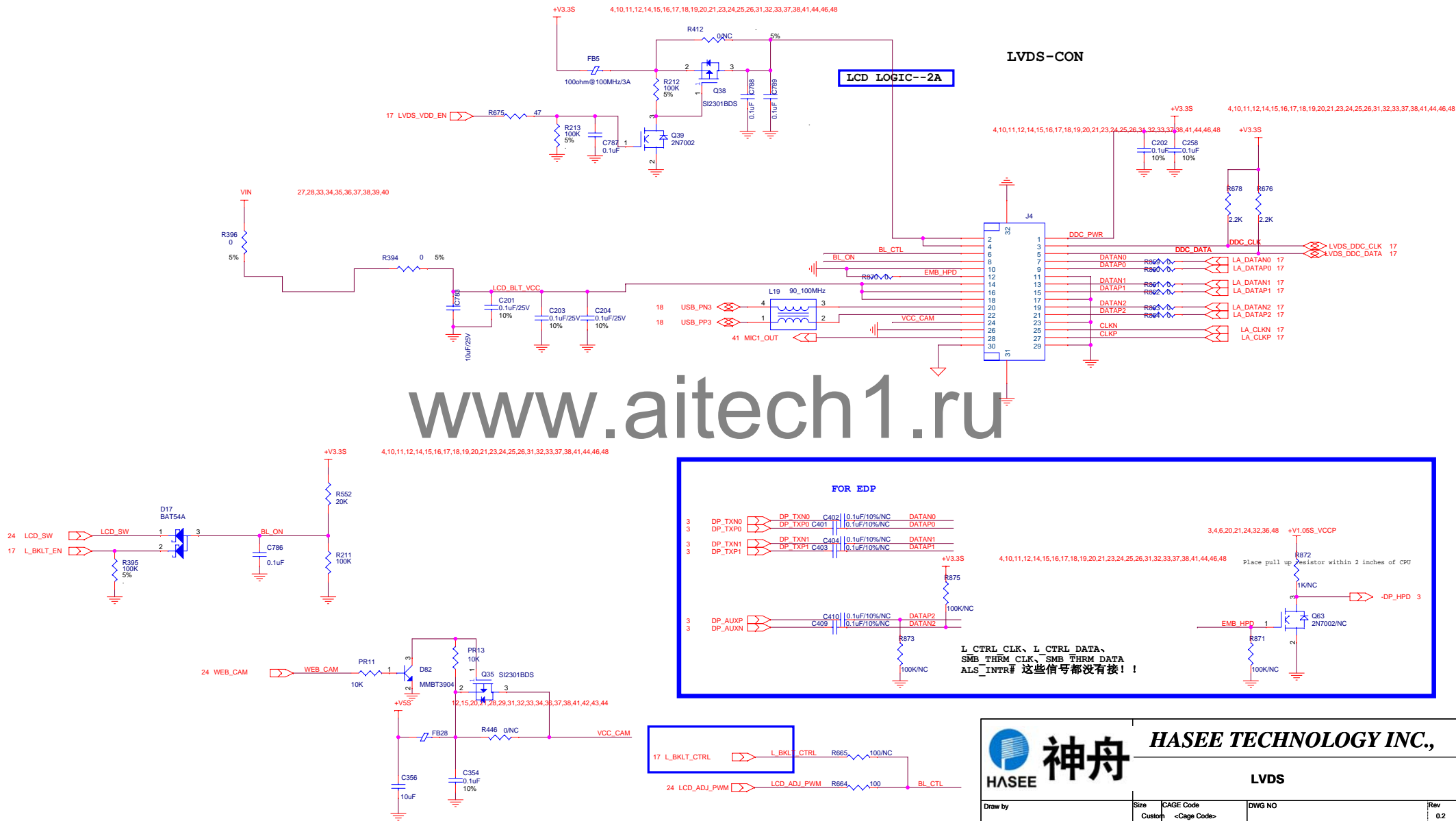
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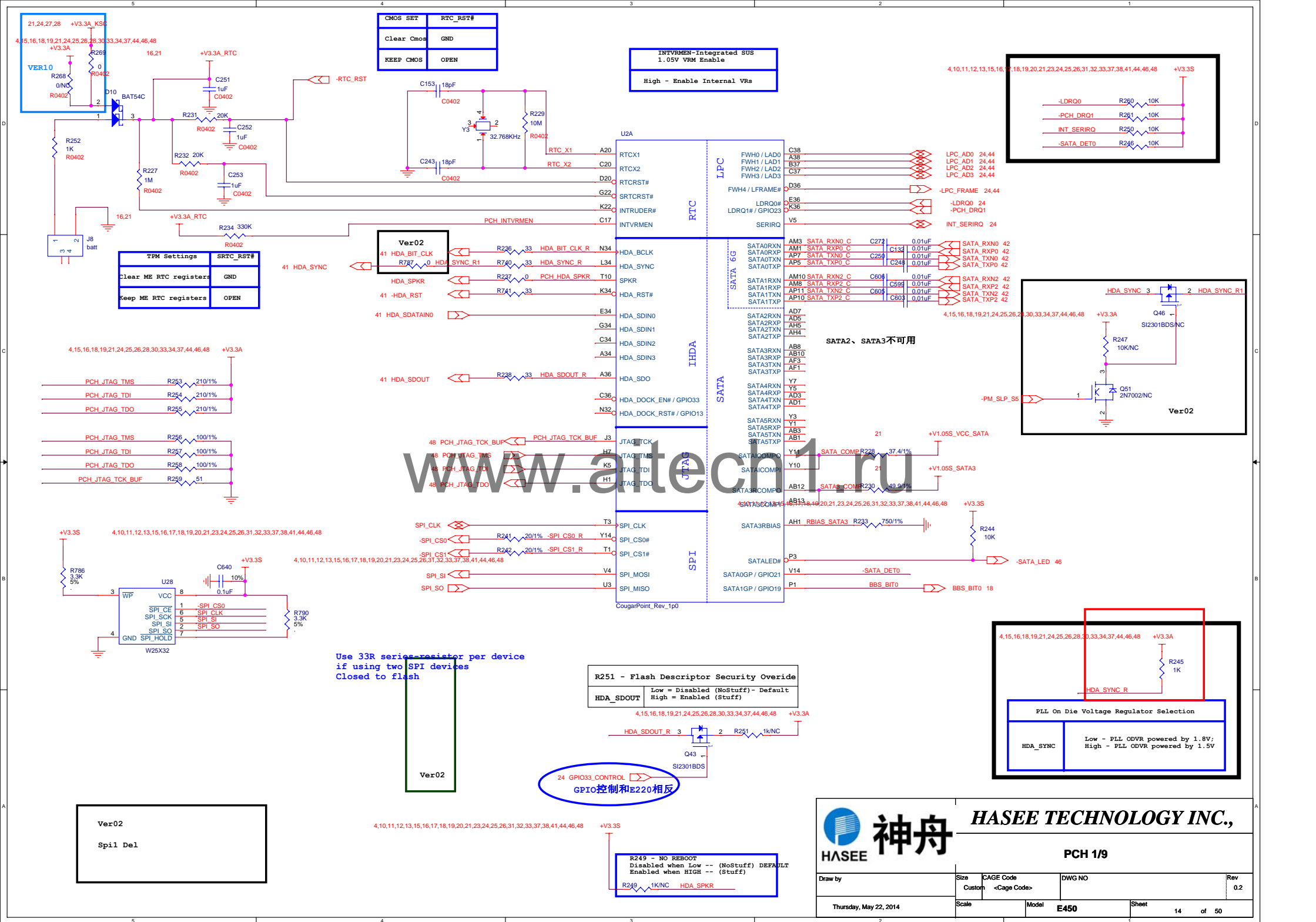
**DIMM 1**

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Thursday, May 22, 2014	Scale	Model <b>E450</b>	Sheet 11	of 50



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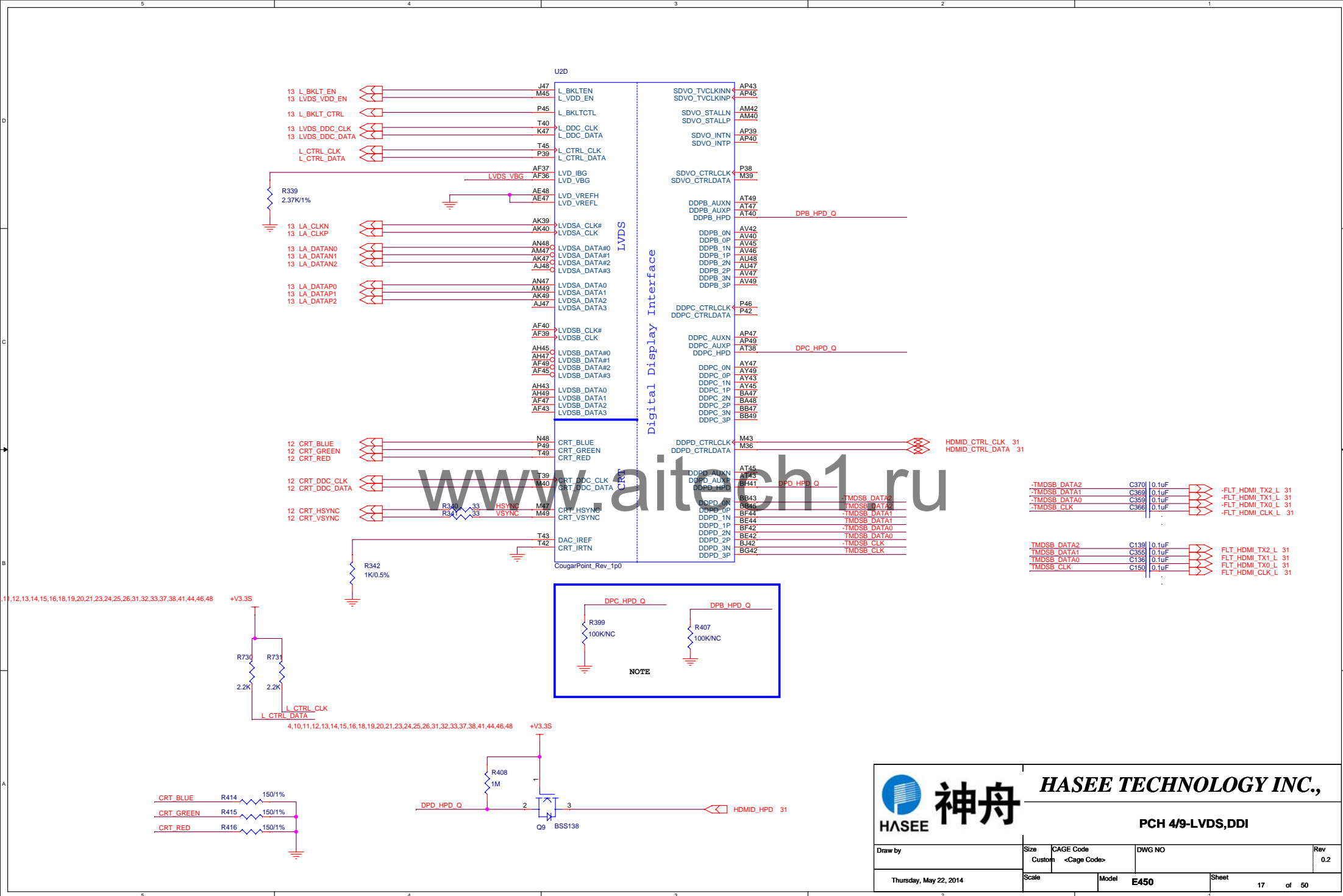


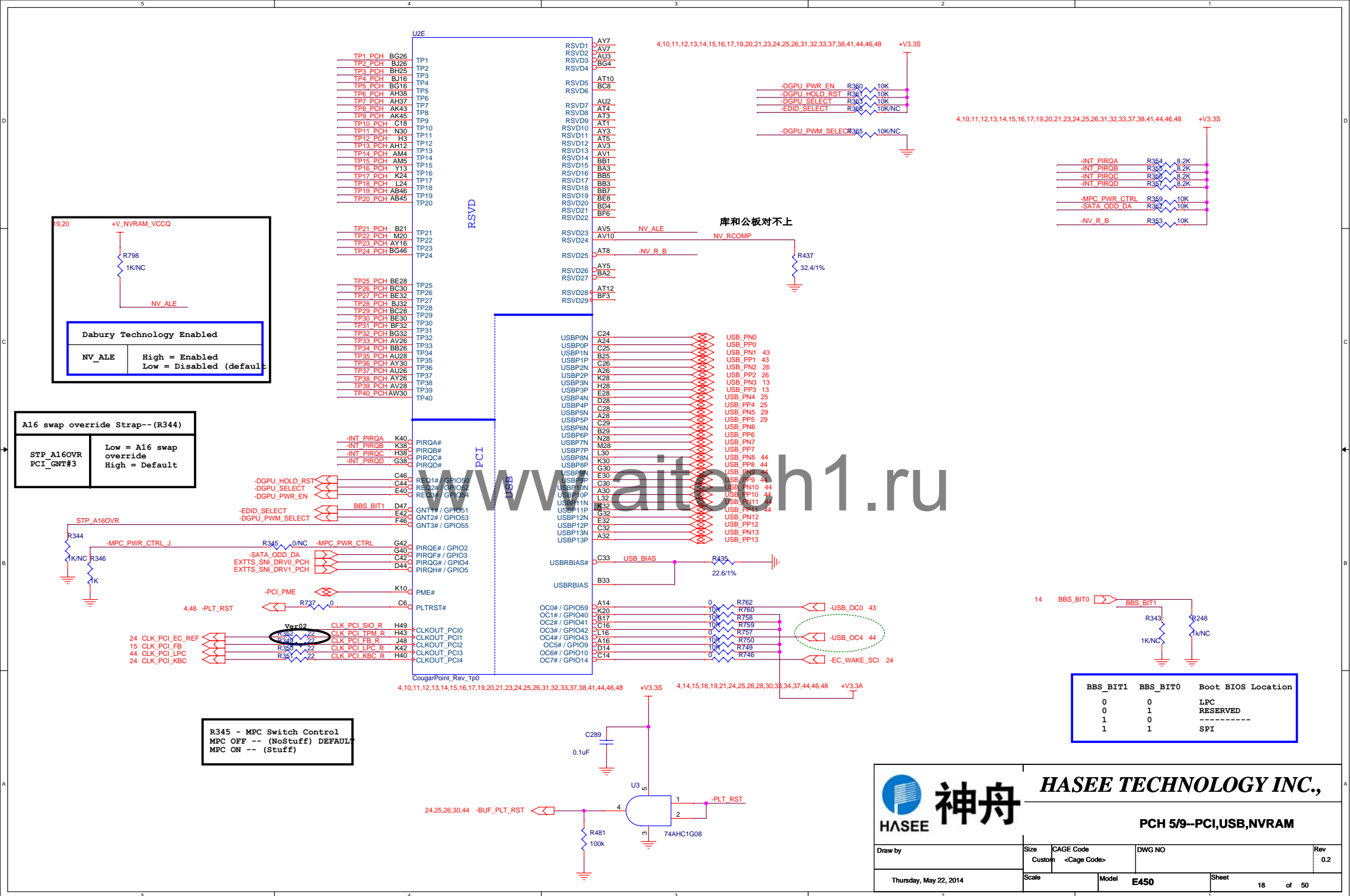




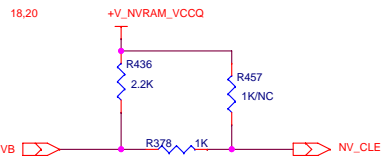




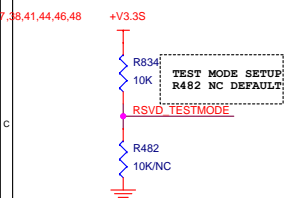




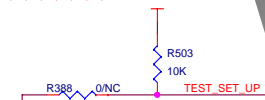
PLACE R378 CLOSE TO THE BRANCHING POINT  
( TO CPT and NVRAM CONNECTOR)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



4,10,11,12,13,14,15,16,17,18,20,21,23,24,25,26,31,32,33,37,38,41,44,46,48

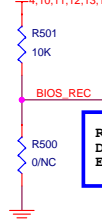


Configurable CPU output buffer	
TEST_SET_UP	High = Strong (Default) Low = Weak

4,14,15,16,18,21,24,25,26,28,30,33,34,37,44,46,48



4,10,11,12,13,14,15,16,17,18,20,21,23,24,25,26,31,32,33,37,38,41,44,46,48



R500 - BIOS RECOVERY  
DISABLE -- (NC) DEFAULT (high)  
ENABLE -- (STUFF) low

4,10,11,12,13,14,15,16,17,18,20,21,23,24,25,26,31,32,33,37,38,41,44,46,48

4,10,11,12,13,14,15,16,17,18,20,21,23,24,25,26,31,32,33,37,38,41,44,46,48



R504 - SGPIO  
(NC) DEFAULT

24 -EC\_EXTSMI  
24 -EC\_RUNTIME\_SCI  
26 -HOST\_ALERT1  
23 -STP\_PCI  
24 -CRIT\_TEMP\_REP

S\_GPIO R364 100 T7  
A42  
H36  
E38  
C10  
C4  
G2  
U2  
D40  
T5  
E8  
E16  
P8  
K1  
K4  
V8  
M5  
N2  
M3  
V13  
V3  
D6  
GPIO0  
GPIO1  
GPIO6  
GPIO7  
GPIO8  
LAN\_PHY\_PWR\_CTRL / GPIO12  
GPIO15  
SATA4GP / GPIO16  
TACH0 / GPIO17  
SCLOCK / GPIO22  
GPIO24 / MEM\_LED  
GPIO27  
GPIO28  
STP\_PC# / GPIO34  
GPIO35  
SATA2GP / GPIO36  
SATA3GP / GPIO37  
SLOAD / GPIO38  
SDATAOUT0 / GPIO39  
SDATAOUT1 / GPIO48  
SATA5GP / GPIO49  
GPIO57

GPIO

CPU/MISC

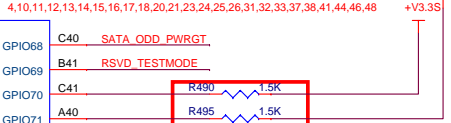
NCTF

A4  
A44  
A45  
A46  
A5  
A6  
B3  
B47  
BD1  
BD49  
BE1  
BE49  
BF1  
BF49  
VSS\_NCTF\_1  
VSS\_NCTF\_2  
VSS\_NCTF\_3  
VSS\_NCTF\_4  
VSS\_NCTF\_5  
VSS\_NCTF\_6  
VSS\_NCTF\_7  
VSS\_NCTF\_8  
VSS\_NCTF\_9  
VSS\_NCTF\_10  
VSS\_NCTF\_11  
VSS\_NCTF\_12  
VSS\_NCTF\_13  
VSS\_NCTF\_14  
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VSS\_NCTF\_32  
CougarPoint\_Rev\_1p0

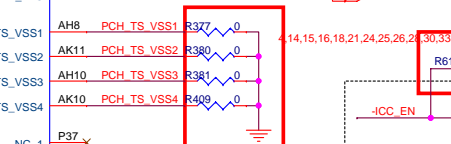
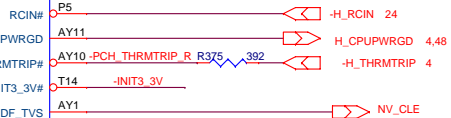
BMBUSY# / GPIO0  
TACH1 / GPIO1  
TACH2 / GPIO6  
TACH3 / GPIO7  
GPIO8  
LAN\_PHY\_PWR\_CTRL / GPIO12  
GPIO15  
SATA4GP / GPIO16  
TACH0 / GPIO17  
SCLOCK / GPIO22  
GPIO24 / MEM\_LED  
GPIO27  
GPIO28  
STP\_PC# / GPIO34  
GPIO35  
SATA2GP / GPIO36  
SATA3GP / GPIO37  
SLOAD / GPIO38  
SDATAOUT0 / GPIO39  
SDATAOUT1 / GPIO48  
SATA5GP / GPIO49  
GPIO57

A20GATE  
PECI  
RCIN#  
AY11  
AY10\_PCH\_THRMTRIP\_R R375 392  
T14  
AY1  
AH8\_PCH\_TS\_VSS1 R377 0  
AH11\_PCH\_TS\_VSS2 R380 0  
AH10\_PCH\_TS\_VSS3 R381 0  
AH10\_PCH\_TS\_VSS4 R409 0  
P37  
BG2  
BG48  
BH3  
BH47  
BJ4  
BJ44  
BJ45  
BJ46  
BJ5  
BJ6  
C2  
C48  
D1  
D49  
E1  
E49  
F1  
F49

4,10,11,12,13,14,15,16,17,18,20,21,23,24,25,26,31,32,33,37,38,41,44,46,48



P4  
AU16 H\_PECI\_R R372 0/NC  
P5  
AY11  
AY10\_PCH\_THRMTRIP\_R R375 392  
T14  
AY1



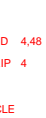
NC\_1  
BG2  
BG48  
BH3  
BH47  
BJ4  
BJ44  
BJ45  
BJ46  
BJ5  
BJ6  
C2  
C48  
D1  
D49  
E1  
E49  
F1  
F49

VSS\_NCTF\_15  
VSS\_NCTF\_16  
VSS\_NCTF\_17  
VSS\_NCTF\_18  
VSS\_NCTF\_19  
VSS\_NCTF\_20  
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VSS\_NCTF\_28  
VSS\_NCTF\_29  
VSS\_NCTF\_30  
VSS\_NCTF\_31  
VSS\_NCTF\_32  
CougarPoint\_Rev\_1p0

4,10,11,12,13,14,15,16,17,18,20,21,23,24,25,26,31,32,33,37,38,41,44,46,48



P4  
AU16 H\_PECI\_R R372 0/NC  
P5  
AY11  
AY10\_PCH\_THRMTRIP\_R R375 392  
T14  
AY1



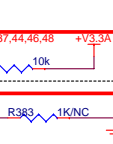
NC\_1  
BG2  
BG48  
BH3  
BH47  
BJ4  
BJ44  
BJ45  
BJ46  
BJ5  
BJ6  
C2  
C48  
D1  
D49  
E1  
E49  
F1  
F49

VSS\_NCTF\_15  
VSS\_NCTF\_16  
VSS\_NCTF\_17  
VSS\_NCTF\_18  
VSS\_NCTF\_19  
VSS\_NCTF\_20  
VSS\_NCTF\_21  
VSS\_NCTF\_22  
VSS\_NCTF\_23  
VSS\_NCTF\_24  
VSS\_NCTF\_25  
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VSS\_NCTF\_28  
VSS\_NCTF\_29  
VSS\_NCTF\_30  
VSS\_NCTF\_31  
VSS\_NCTF\_32  
CougarPoint\_Rev\_1p0

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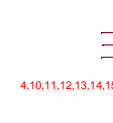
P4  
AU16 H\_PECI\_R R372 0/NC  
P5  
AY11  
AY10\_PCH\_THRMTRIP\_R R375 392  
T14  
AY1



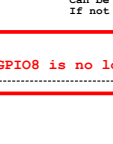
NC\_1  
BG2  
BG48  
BH3  
BH47  
BJ4  
BJ44  
BJ45  
BJ46  
BJ5  
BJ6  
C2  
C48  
D1  
D49  
E1  
E49  
F1  
F49

VSS\_NCTF\_15  
VSS\_NCTF\_16  
VSS\_NCTF\_17  
VSS\_NCTF\_18  
VSS\_NCTF\_19  
VSS\_NCTF\_20  
VSS\_NCTF\_21  
VSS\_NCTF\_22  
VSS\_NCTF\_23  
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VSS\_NCTF\_28  
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VSS\_NCTF\_32  
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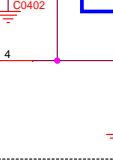
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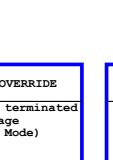
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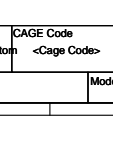
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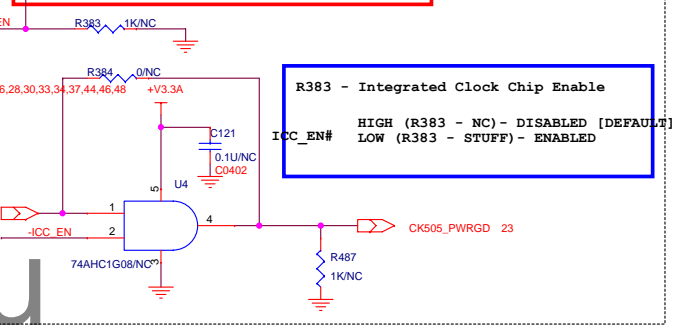
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4,10,11,12,13,14,15,16,17,18,20,21,23,24,25,26,31,32,33,37,38,41,44,46,48

GPIO27:  
Can be configured as wake input to allow wakes from Deep Sleep.  
If not used then use 8.2-kΩ to 10-kΩ pull-down to GND

GPIO8 is no longer ICC strap




PLL ON DIE VR ENABLE  
ENABLED -- HIGH (R385 NC) DEFAULT  
DISABLED -- LOW (R385 STUFF)

FDI\_OVRVLGTG R386 1K1%NC  
R488 100K  
R494 100K  
R499 100K  
R501 10K  
R505 1K1%  
R506 10K  
R507 0/NC

FDI TERMINATION VOLTAGE OVERRIDE  
GPIO37 (FDI\_OVRVLGTG) LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

DMI TERMINATION VOLTAGE OVERRIDE  
GPIO36 (SATA\_ODD\_PRSNRT#) LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT



HASEE

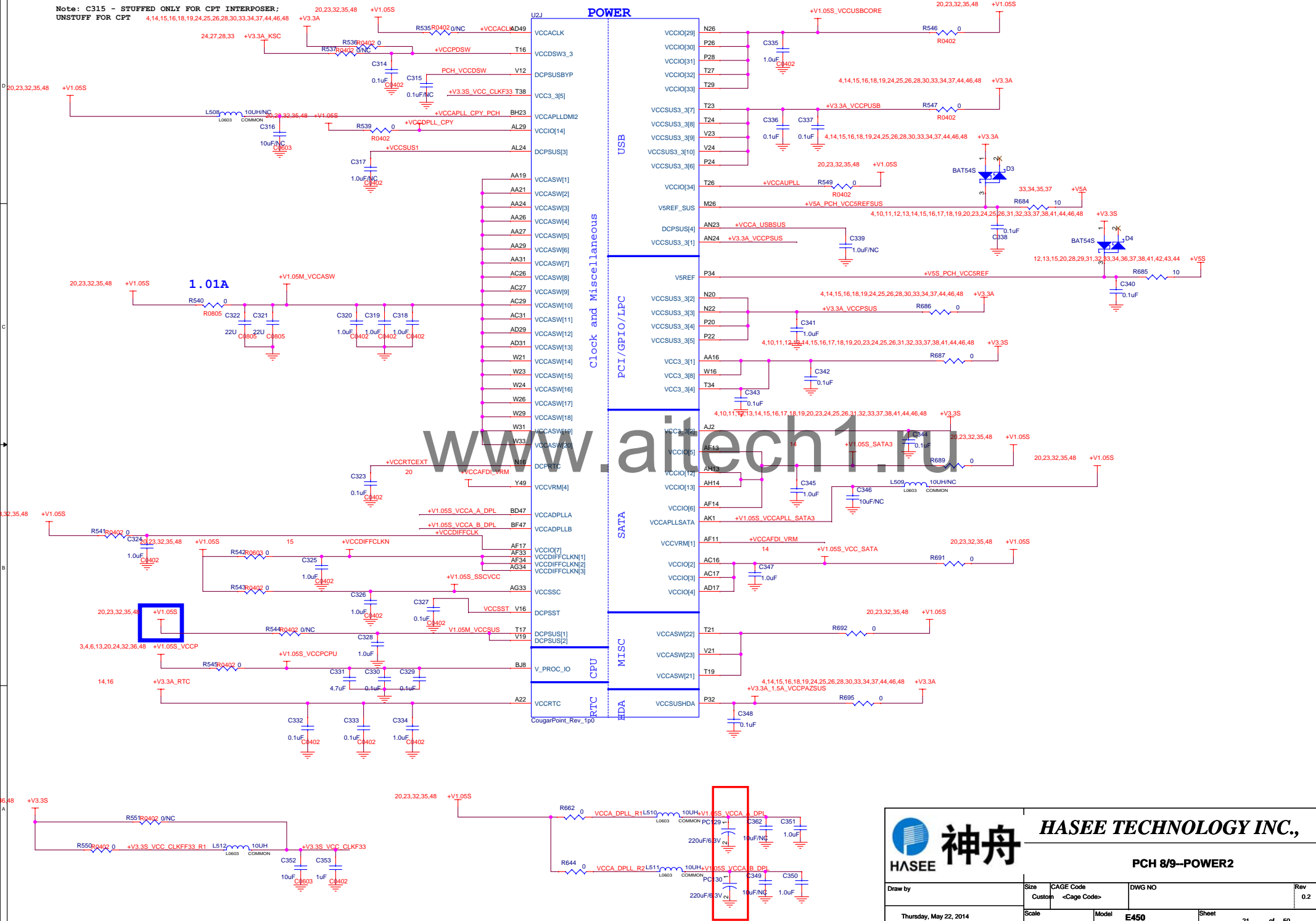
HASEE TECHNOLOGY INC.,

PCH 6/9-GPIO,VSS

Draw by	Size	CAGE Code	DWG NO	Rev
Thursday, May 22, 2014	Custom	<Cage Code>	E120	0.2
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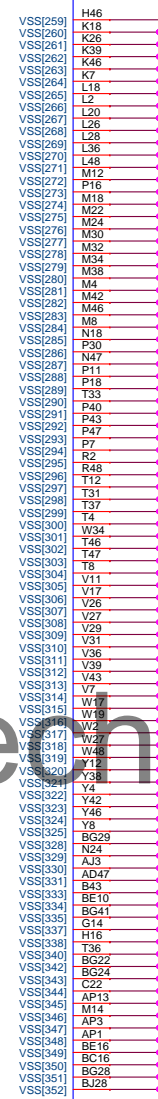
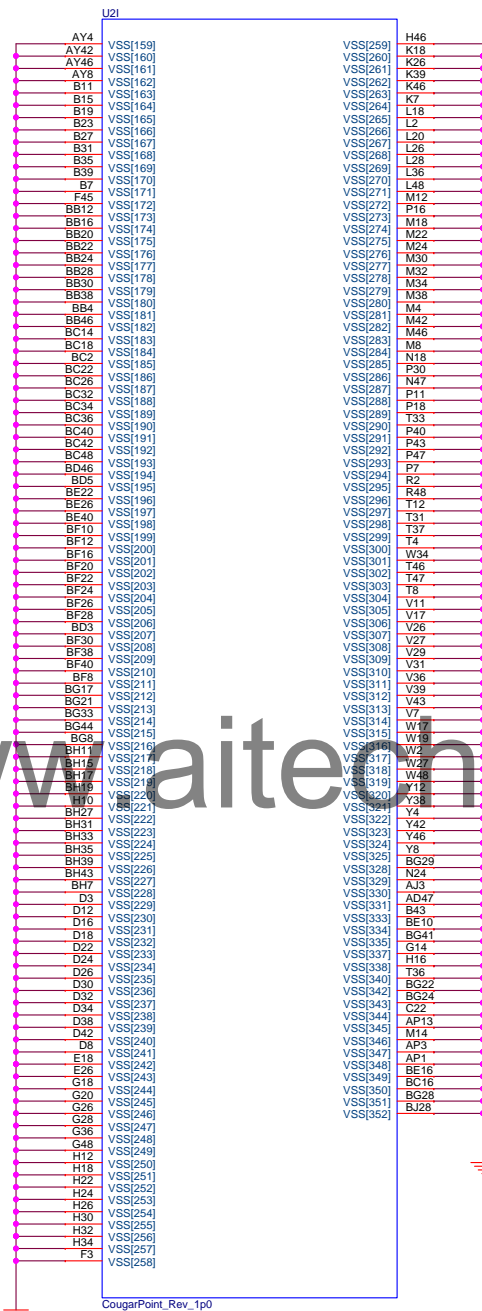
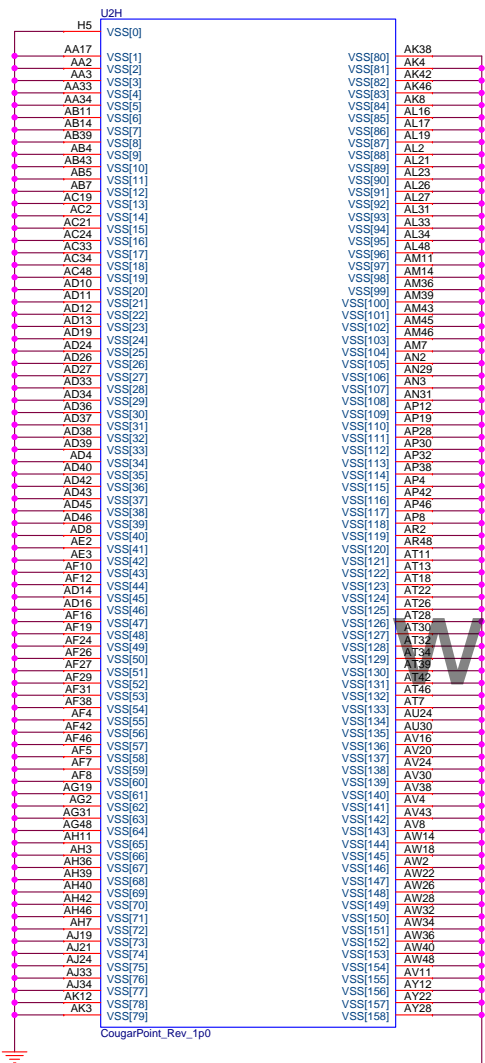
Note: C315 - STUFFED ONLY FOR CPT INTERPOSER;  
UNSTUFF FOR CPT 4.14,15,16,18,19,24,25,26,28,30,33,34,37,44,46




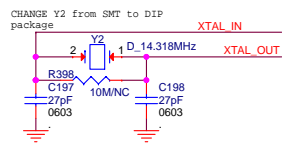
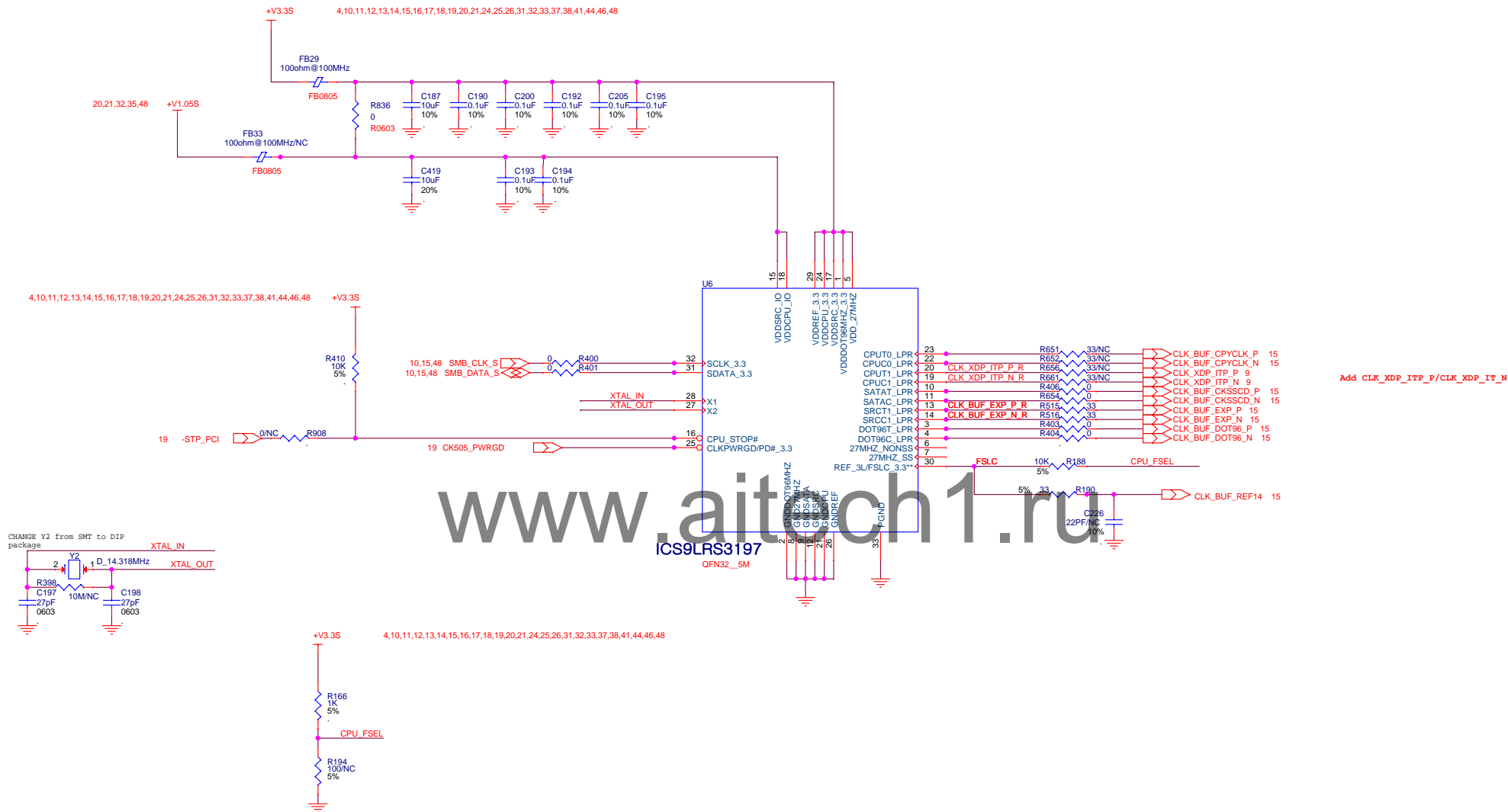
**HASEE TECHNOLOGY INC.,**

**PCH 8/9--POWER2**

Draw by	Size Custom	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model	E450	Sheet




 <b>HASEE 神舟</b>		<b>HASEE TECHNOLOGY INC.,</b>		<b>PCH 9/9--VSS</b>	
Draw by	Size	CAGE Code	DWG NO	Rev	
	Custom	<Cage Code>		0.2	
Thursday, May 22, 2014	Scale	Model	E450	Sheet	22 of 50



CPU frequency setting is 100 MHz

FSLC	CPU
0	133MHZ
1	100MHZ



HASEE 神舟

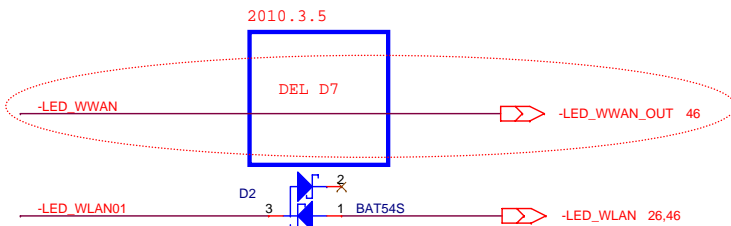
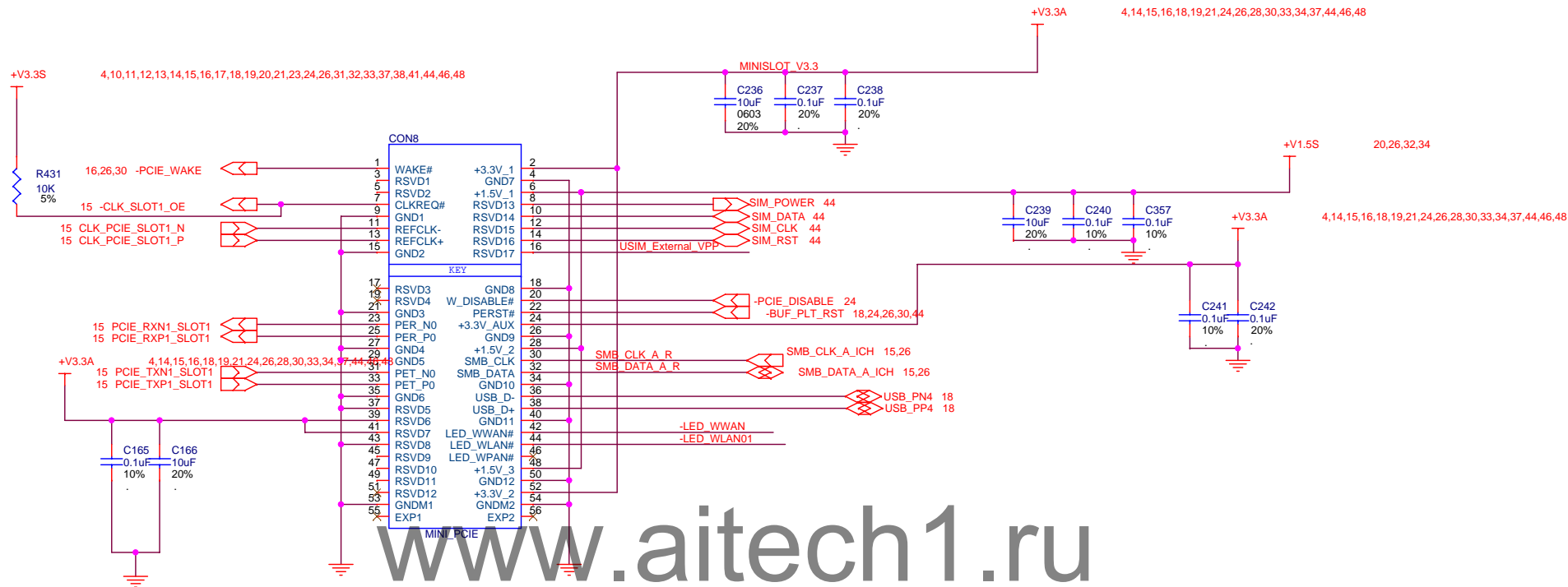
HASEE TECHNOLOGY INC.,


CK505

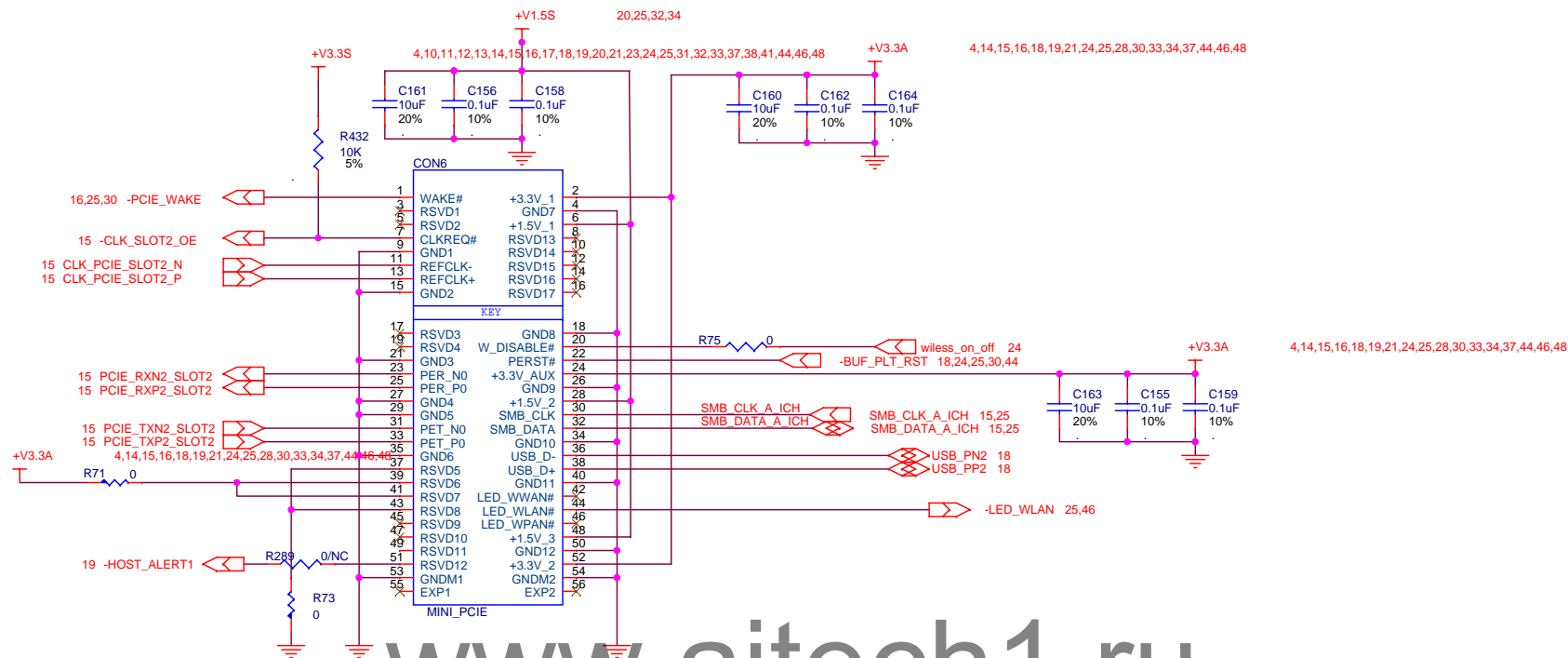
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Thursday, May 22, 2014	Scale	Model	E450	Sheet 23 of 50






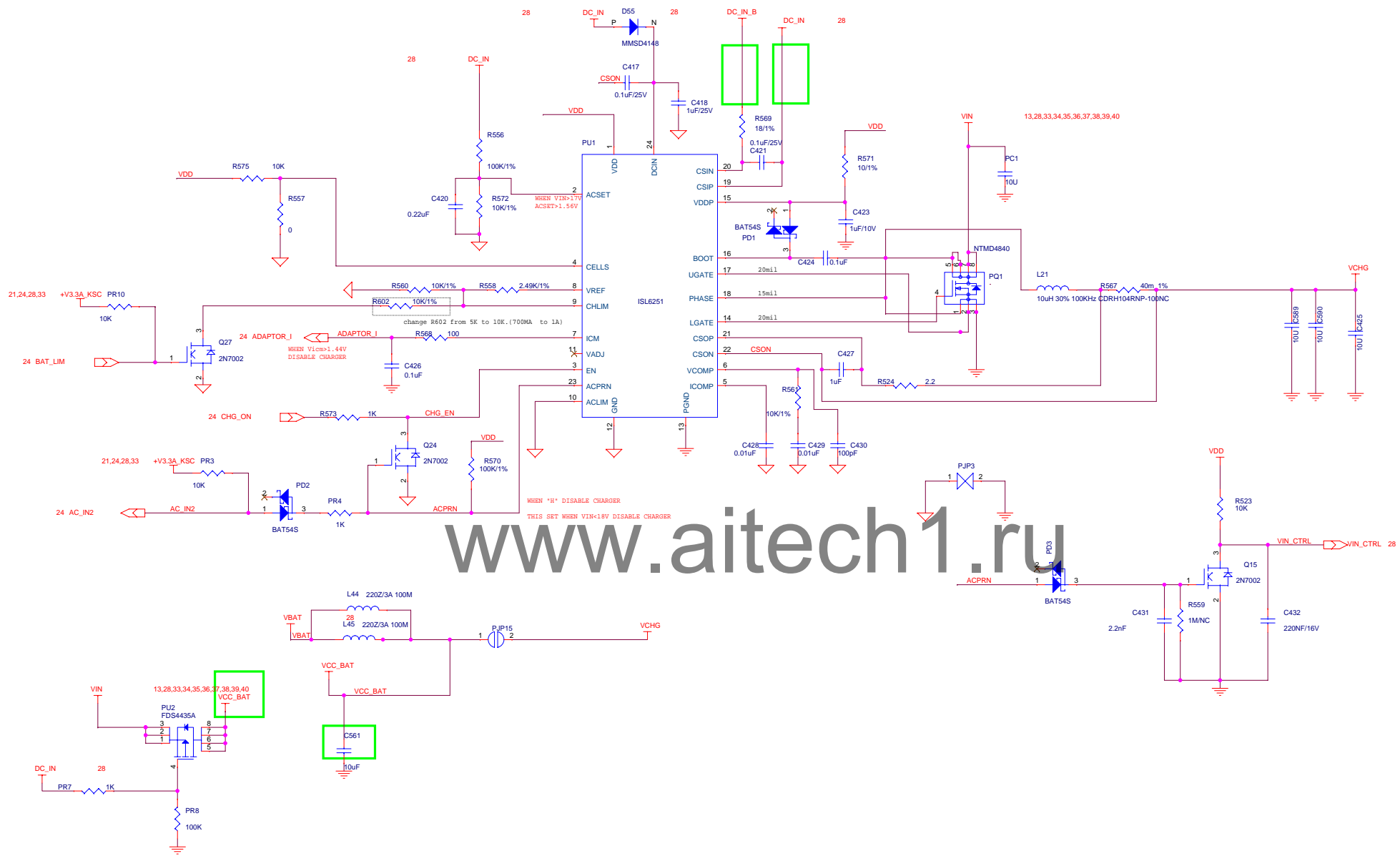


 <b>神舟</b>		<b>HASEE TECHNOLOGY INC.,</b>		
		<b>MiniPCI-E 1</b>		
Draw by	Size B	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model <b>E450</b>	Sheet 25 of 50	




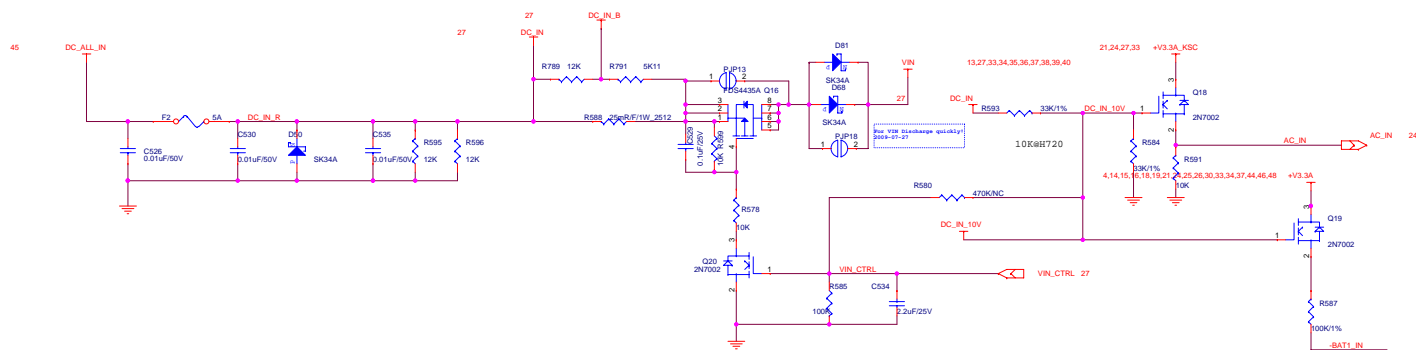
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 <b>神舟</b>		<b>HASEE TECHNOLOGY INC.,</b>	
<b>MiniPCI-E 2</b>			
Draw by Thursday, May 22, 2014	Size B	CAGE Code <Cage Code>	DWG NO E450
Scale		Model E450	Sheet 26 of 50



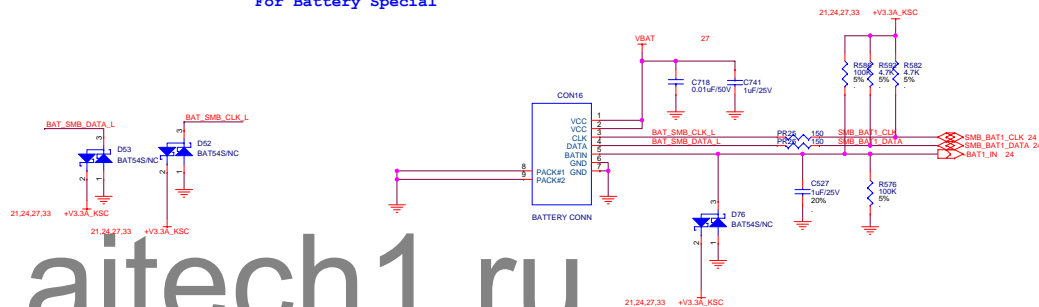
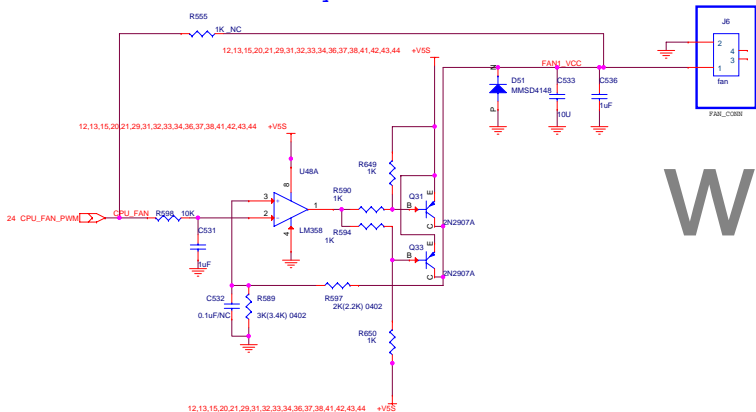
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 <b>神舟</b>		<b>HASEE TECHNOLOGY INC.,</b>	
		<b>CHARGE VR</b>	
Draw by	Size	CAGE Code	DWG NO
	Custom	<Cage Code>	
Thursday, May 22, 2014	Scale	Model	Sheet
		<b>E450</b>	27 of 50



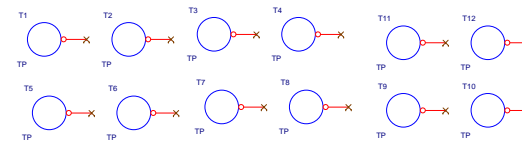
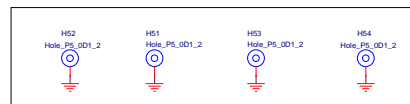
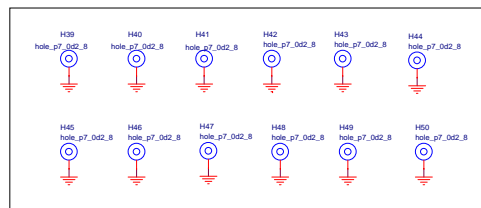
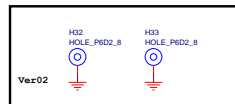
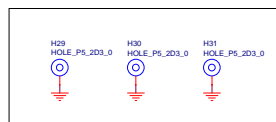
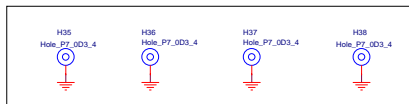
For Battery Special

System FAN connector

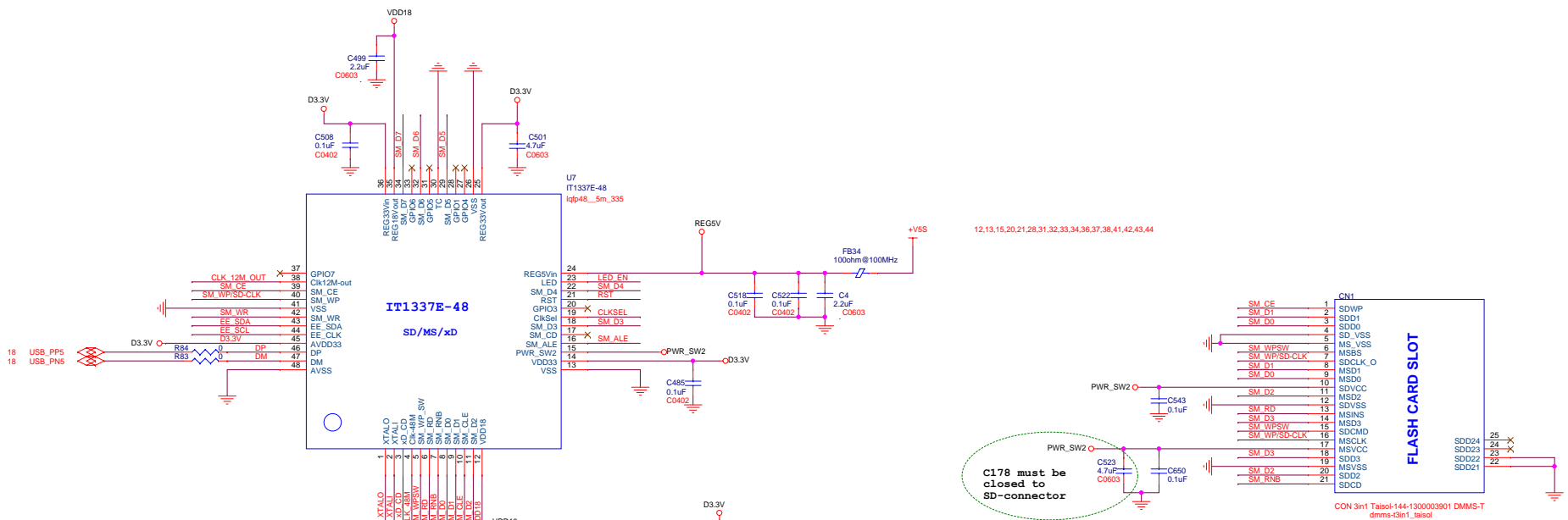


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HOLE

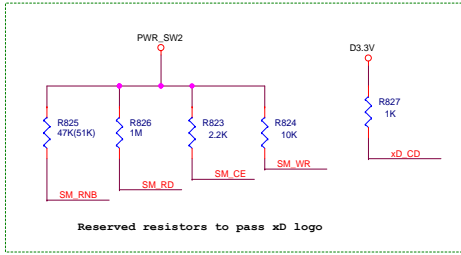
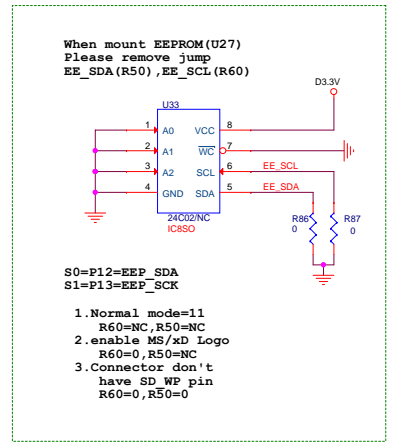


		HASEE TECHNOLOGY INC.,	
		DC-IN FAN BAT	
Draw by	Size	Output	Rev
Thursday, May 22, 2014	Scale	Model	0.2
		E450	28 of 50

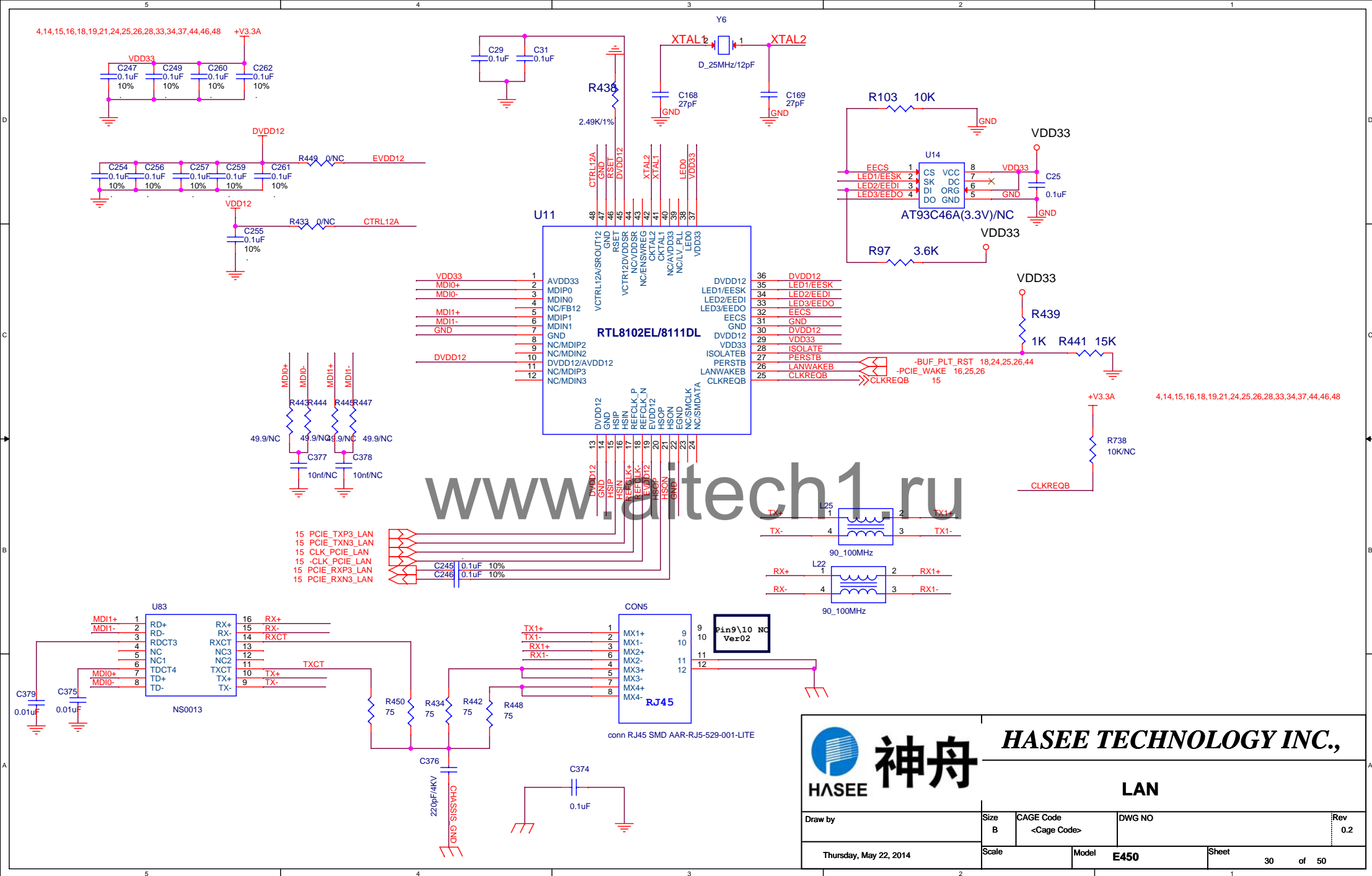


C178 must be closed to SD-connector

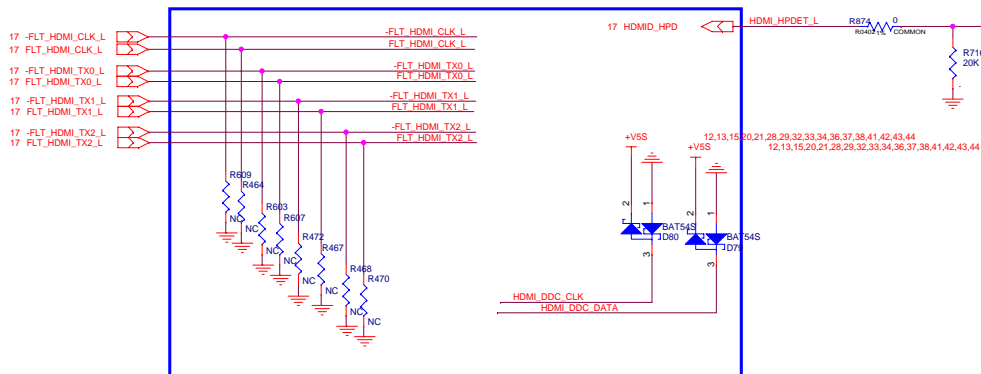
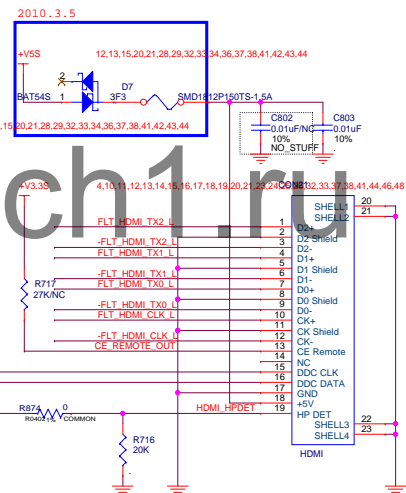
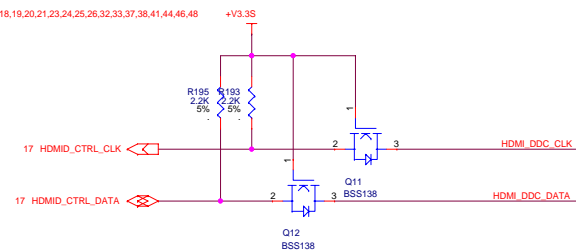
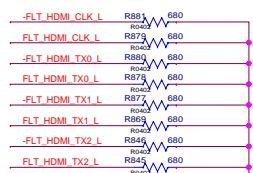
IT1337E-48 PIN MUX			
PINS	SM/xD	SD/MMC	MS
05	SM_WPSW	SD_CMD	MS_BS
06	SM_RD		MS_INS
07	SM_RNB	SD_CD	
08	SM_D0	SD_D0	MS_D0
09	SM_D1	SD_D1	MS_D1
11	SM_D2	SD_D2	MS_D2
18	SM_D3	SD_D3	MS_D3
22	SM_D4	SD_D4	MS_D4
29	SM_D5	SD_D5	MS_D5
32	SM_D6	SD_D6	MS_D6
34	SM_D7	SD_D7	MS_D7
39	SM_CE	SD_WP	
40	SM_WP	SD_CLK	MS_CLK



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\* \* \*

**HASEE TECHNOLOGY INC.,**

## HDMI

Draw by
Thursday, May 22, 2014

Size C	CAGE Code ◀Cage Code▶	DWG NO	Rev 0.2
Scale	Model <b>E450</b>	Sheet 31 of 50	

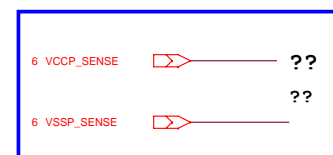
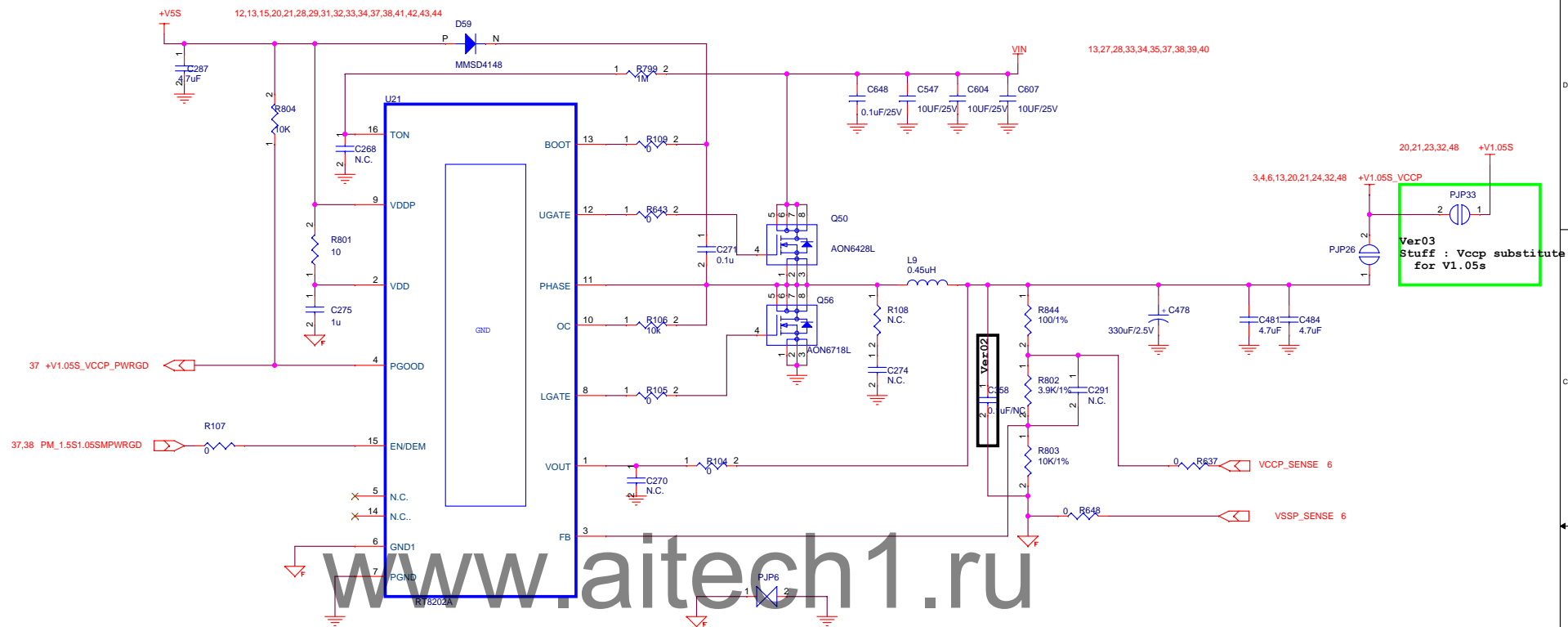





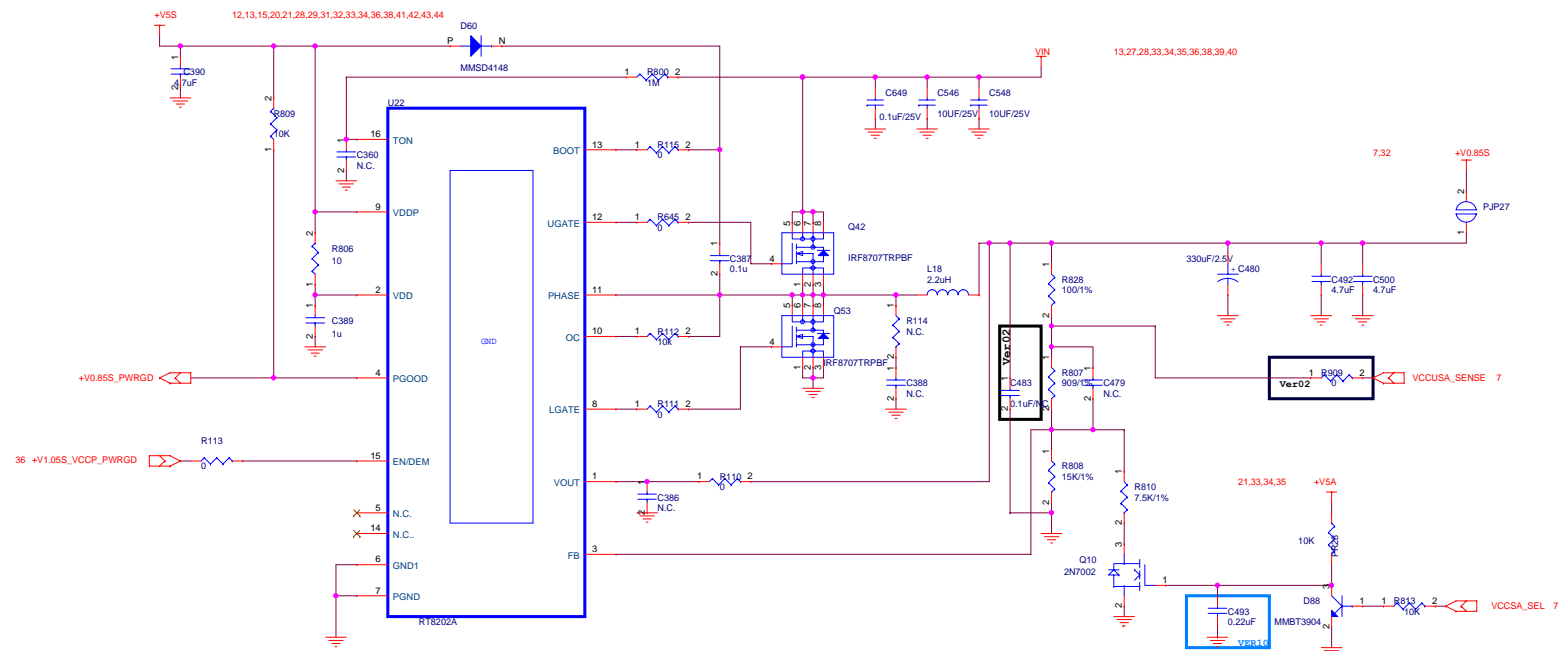




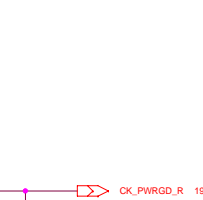
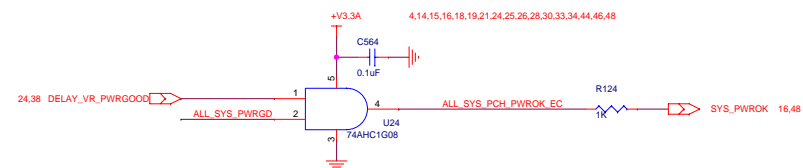
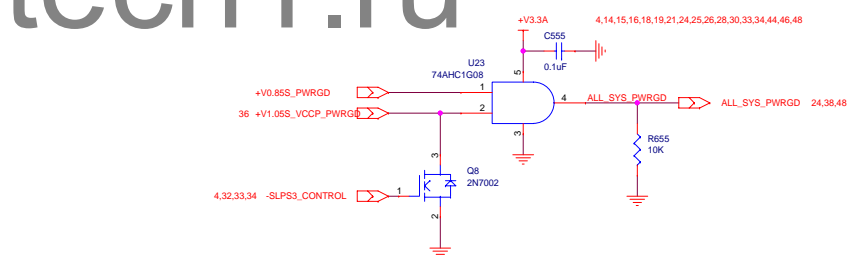
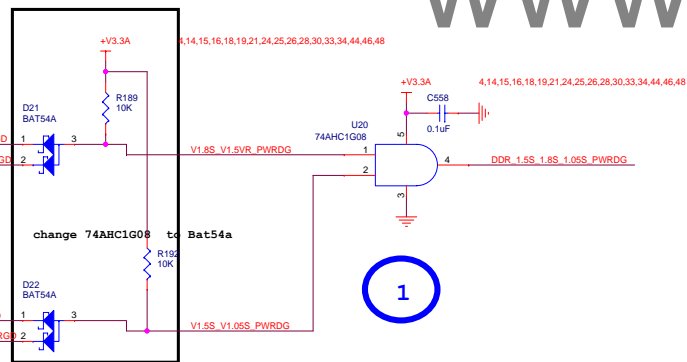




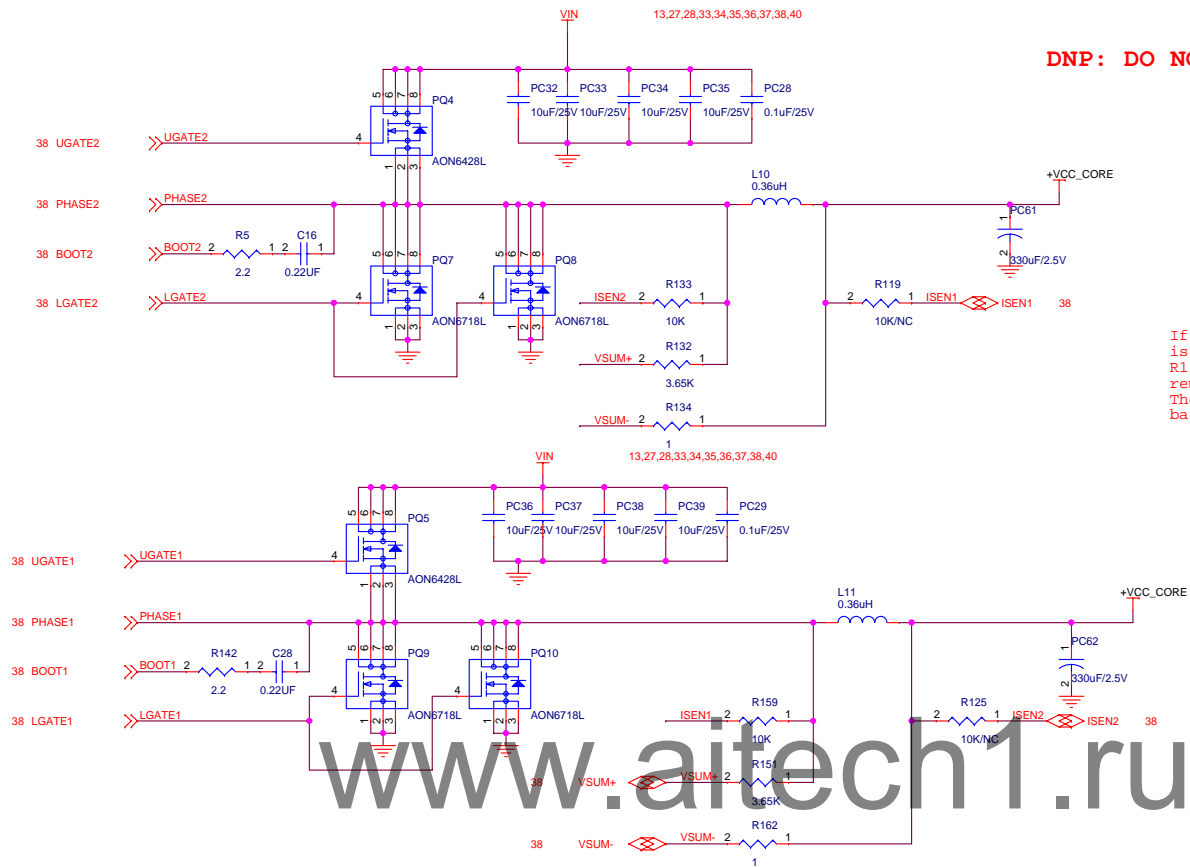
 <b>神舟</b>		<b>HASEE TECHNOLOGY INC.,</b>	
<b>1.05S_VCCP</b>			
Draw by	Size	CAGE Code	DWG NO
	Custom	<Cage Code>	
Thursday, May 22, 2014	Scale	Model	Sheet
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DNP: DO NOT POPULATE

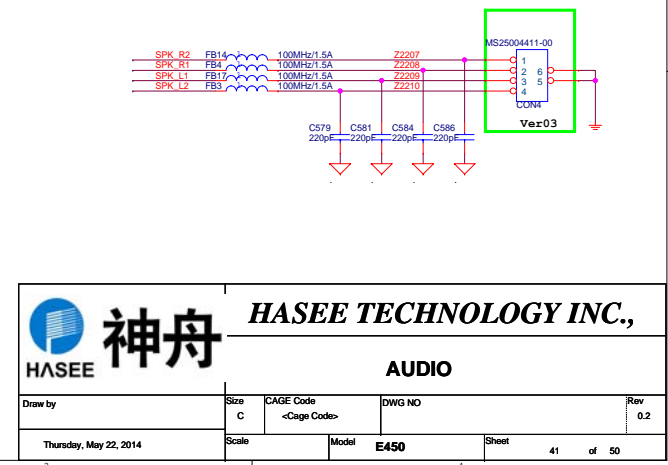
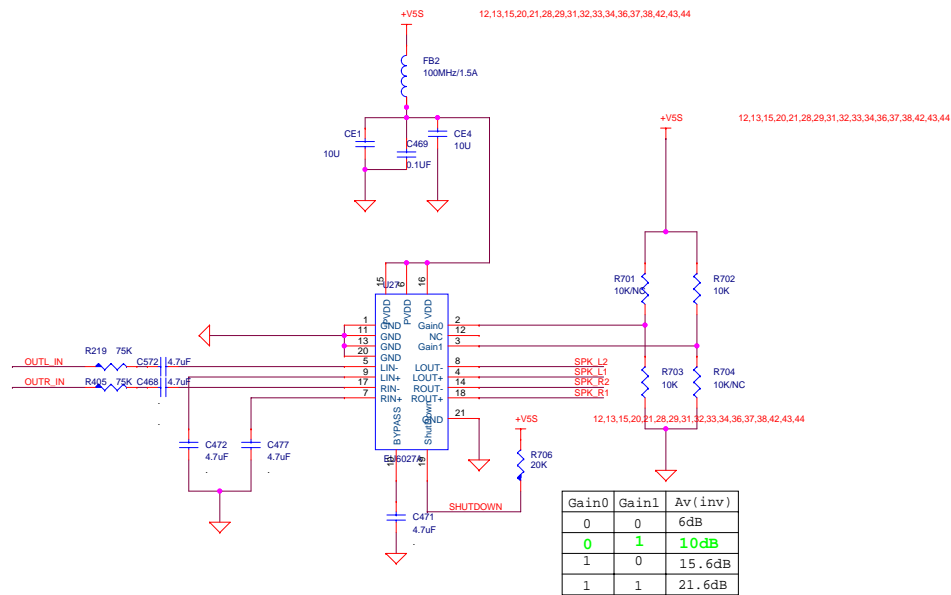
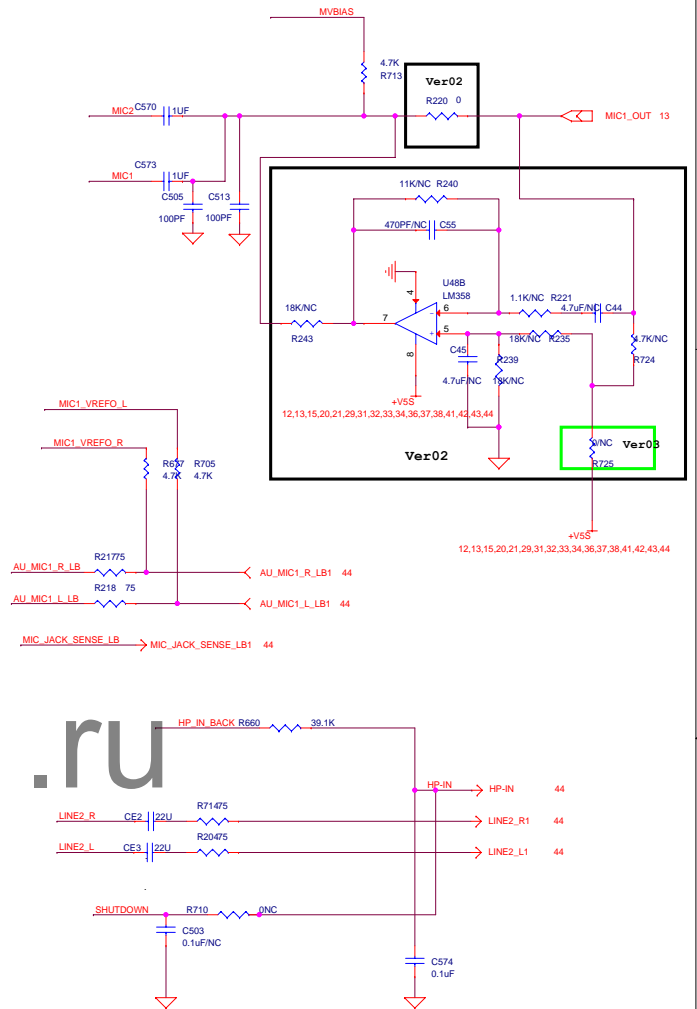
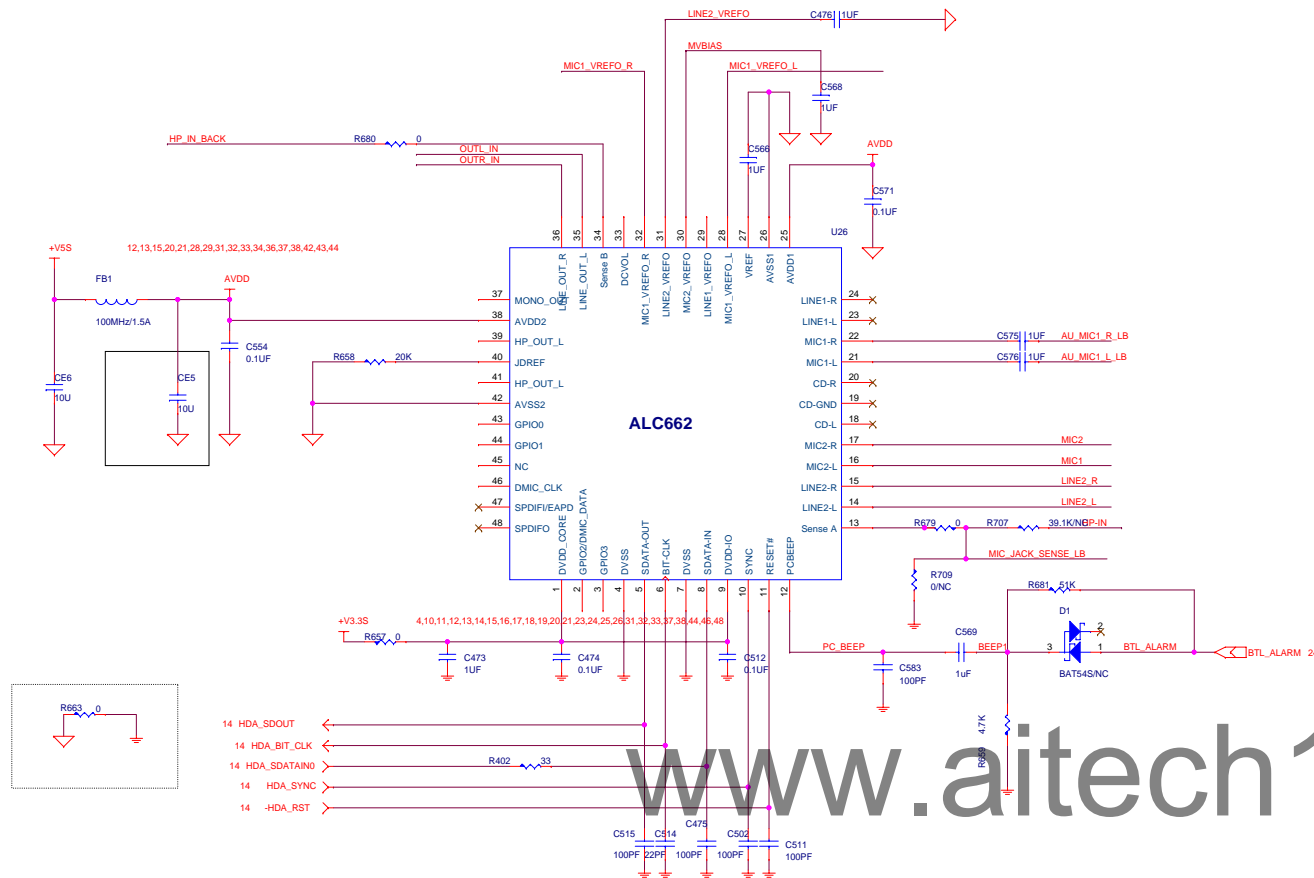
If the layout of each phase to CPU is symmetric. R119, R160, R125, R164, can be removed. They are used for phase current balance adjustment.

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		<b>HASEE TECHNOLOGY INC.,</b>	
		<b>CPU VR2</b>	
Draw by	Size	CAGE Code	DWG NO
	Custom	<Cage Code>	
Thursday, May 22, 2014	Scale	Model	Sheet
		<b>E450</b>	39 of 50

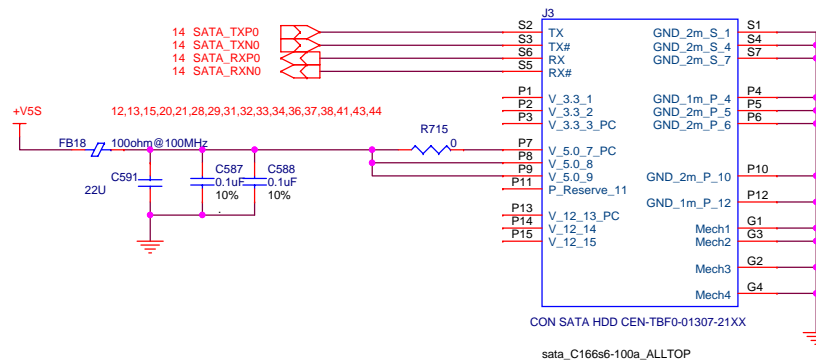






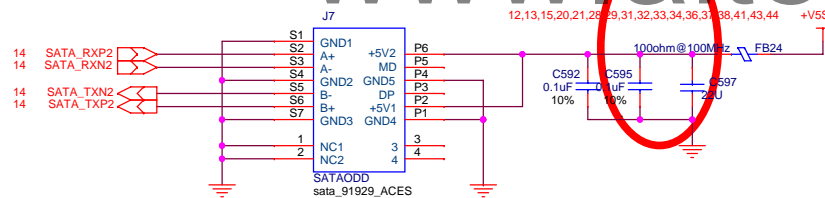
## SATA-HDD

PACKAGE: 同E100  
sata\_C166s6-100a\_ALLTOP



## SATA-ODD

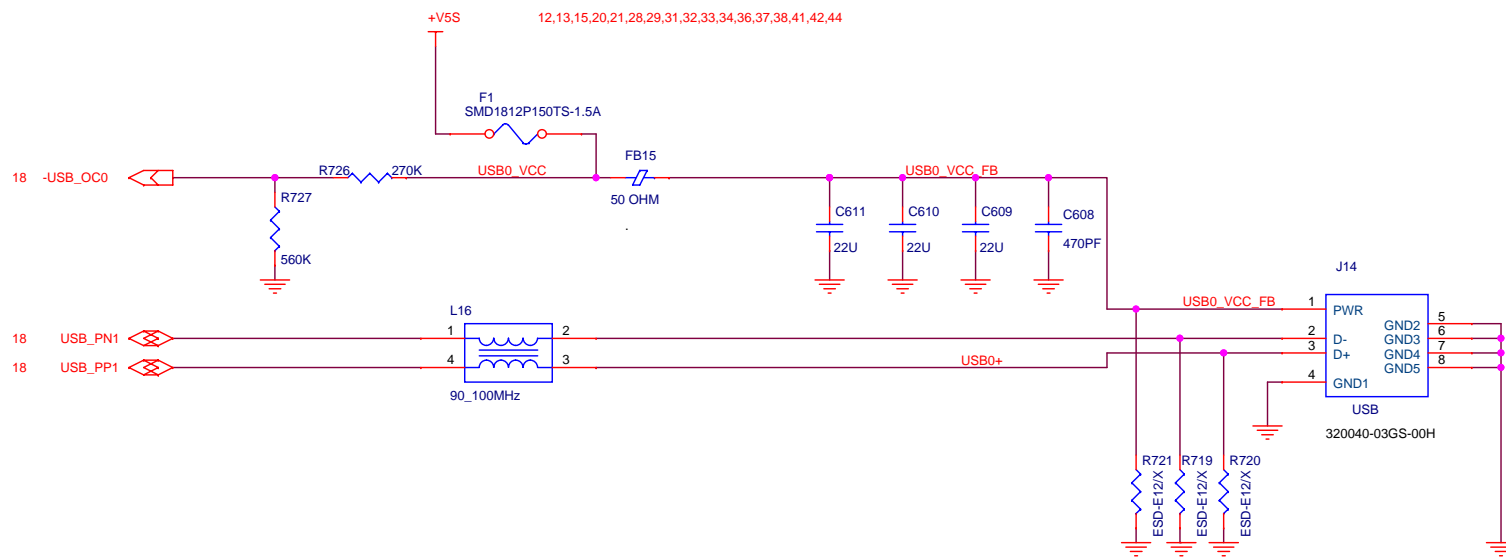
(PACKAGE:sata\_91929\_ACES)




**HASEE TECHNOLOGY INC.,**

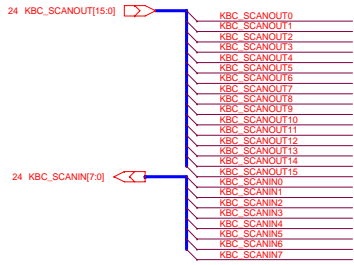
**SATA HDD & ODD**

Draw by	Size Custom	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model <b>E450</b>	Sheet 42 of 50	



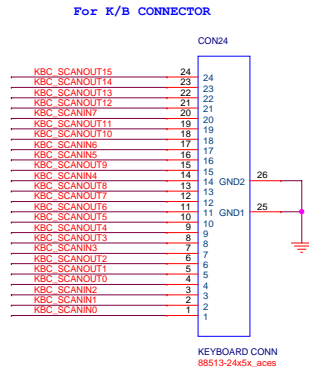
www.aitech1.ru

 <b>神舟</b> HASEE		<b>HASEE TECHNOLOGY INC.,</b>		
		<b>ESATA &amp; USB Ports</b>		
Draw by	Size B	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014	Scale	Model <b>E450</b>	Sheet 43 of 50	



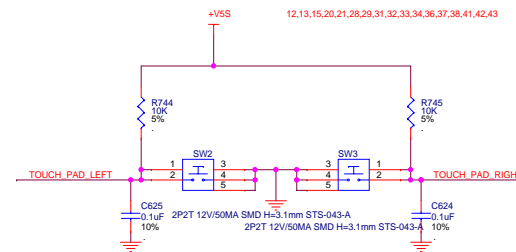
E400

Doking Keyboard.  
(DOK-6129B\_US)



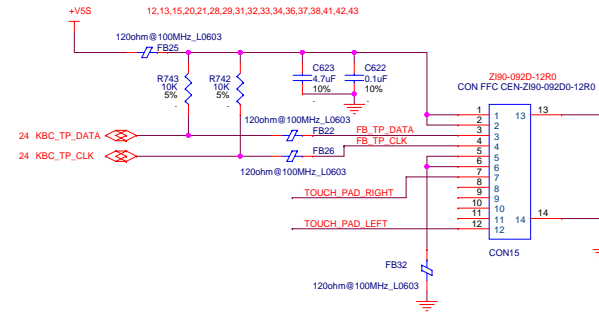
Keyboard-CON

TOUCH PAD LEFT/RIGHT BUTTON

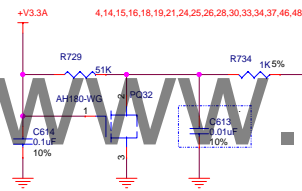


TOUCHPAD (CON15)  
线序已更改同 TM-00372-027  
封装已更改同 E220  
20100629

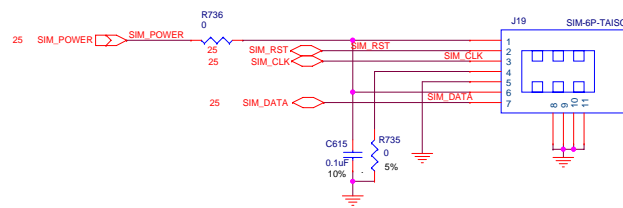
TOUCH PAD CONNECTOR



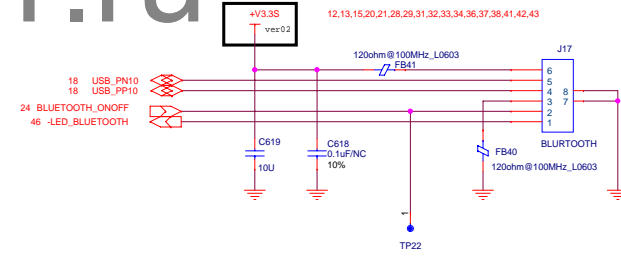
For LID SW



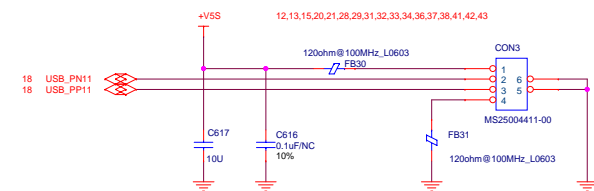
For 3G SIM/UIM CARD



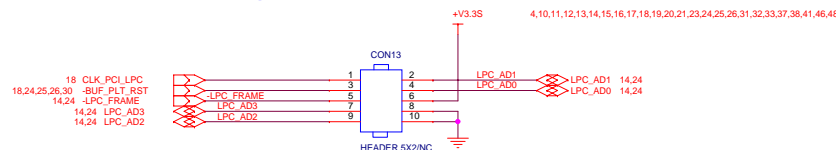
For BLUETOOTH



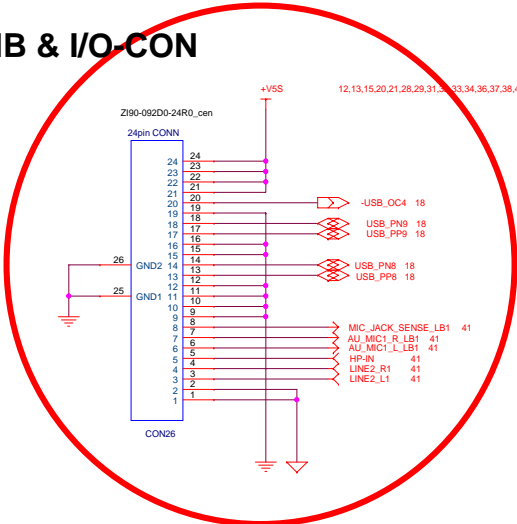
For touch screen




Debug Connector



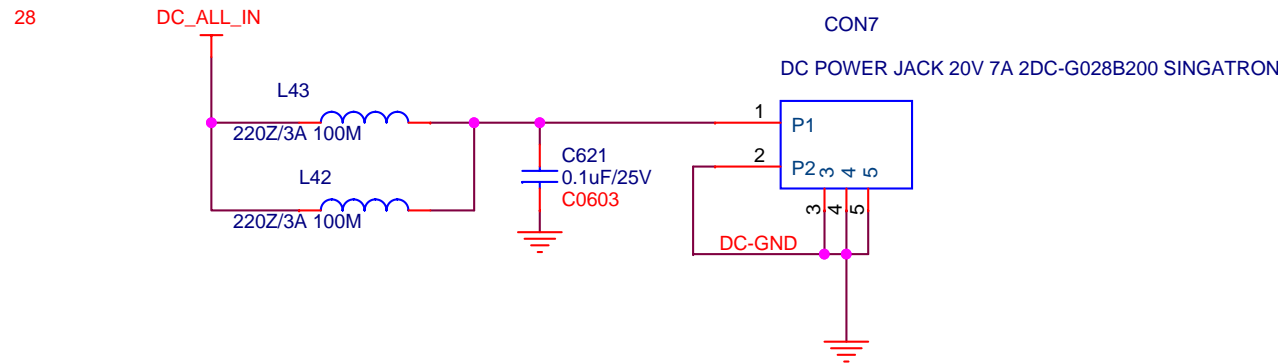
MB & I/O-CON



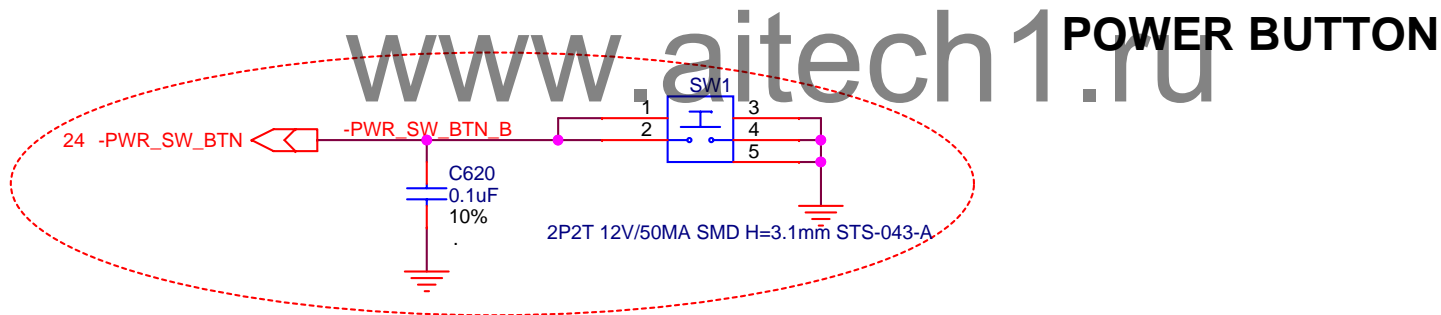
PACKAGE  
ZI90-092D0-24R0\_cen  
朝向

		HASEE TECHNOLOGY INC.,	
Board Connector			
Draw by	Size	CAGE Code	DWG NO
Thursday, May 22, 2014	C	<Cage Code>	Rev 0.2
Scale	Model	E450	Sheet 44 of 50

# DC IN-PORT



# POWER BUTTON



神舟

**HASEE TECHNOLOGY INC.,**

## DC-PORT & POWER-BUTTON

Draw by

Size  
A

CAGE Code

<Cage Code>

DWG NO

Rev  
0.2

Thursday, May 22, 2014

Scale

Model

**E450**

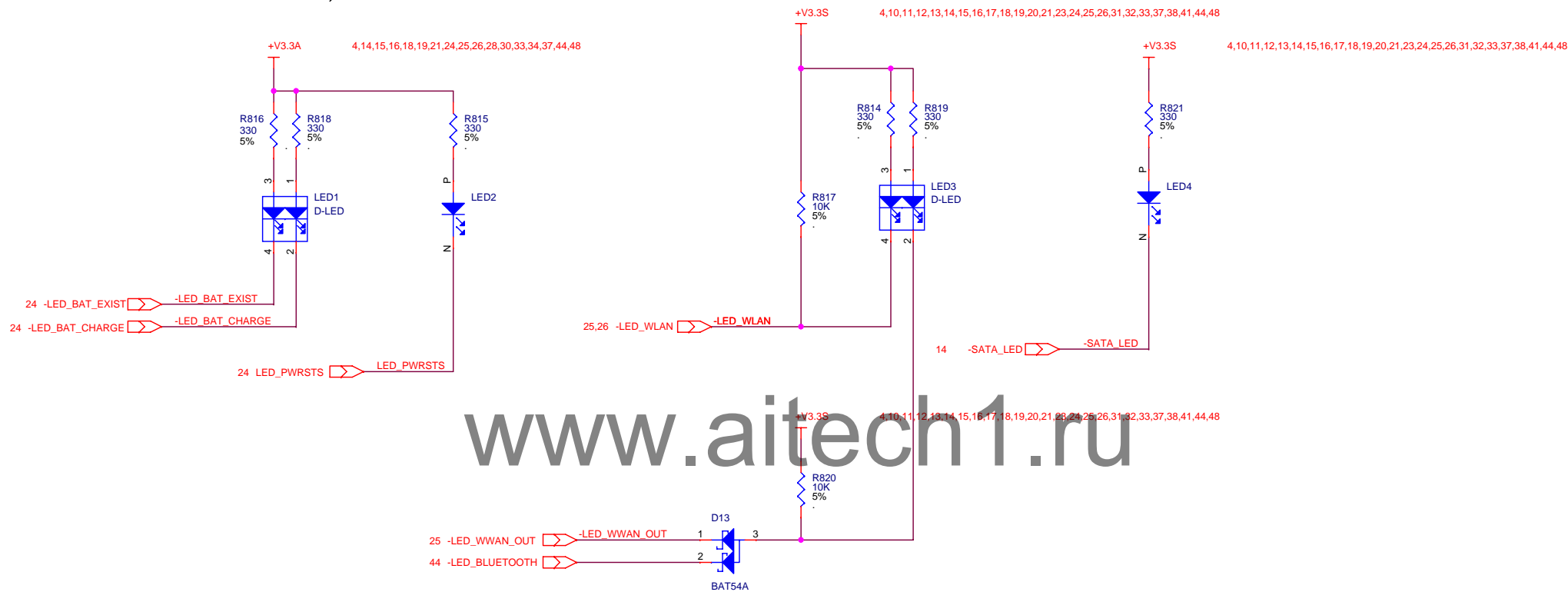
Sheet


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PWRSTS	WLAN	BATT-LED	HDD
LED2	LED3	LED1	LED4

TOP Left Right

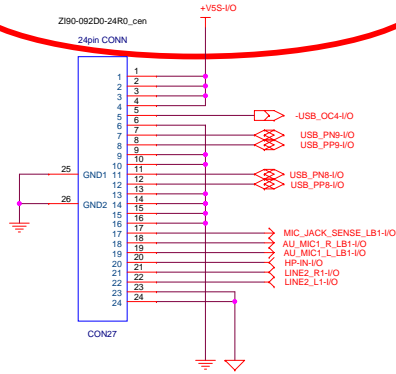
LED



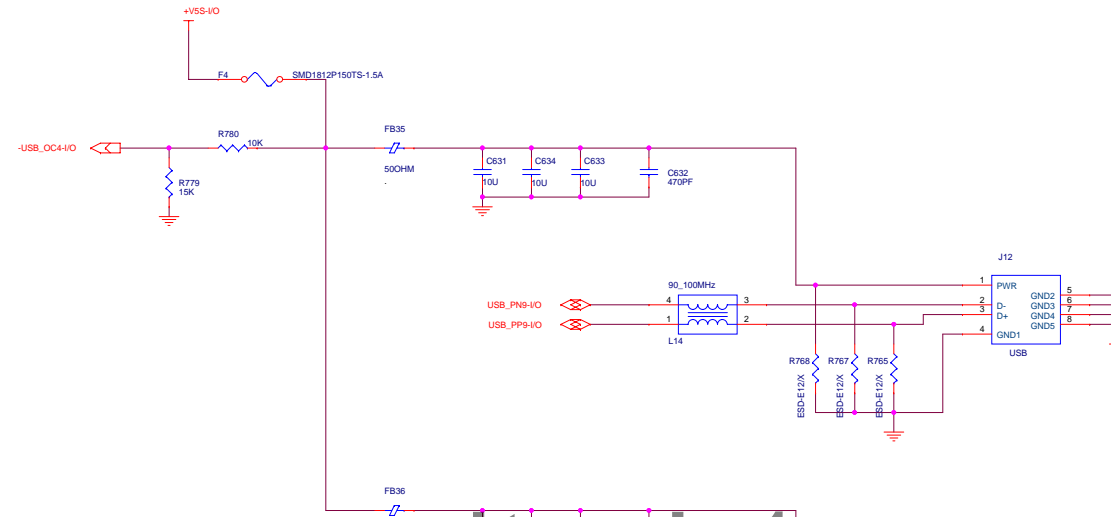
<div><div>HASEE</div></div> <div>神舟</div>		<div>HASEE TECHNOLOGY INC.,</div>			
		LED			
Draw by	Size B	CAGE Code <Cage Code>	DWG NO		Rev 0.2
Thursday, May 22, 2014	Scale	Model	E450	Sheet	46 of 50

I/O & MB-CON  
GND-I/O  
GND\_CODEC-I/O

I/O & MB-CON

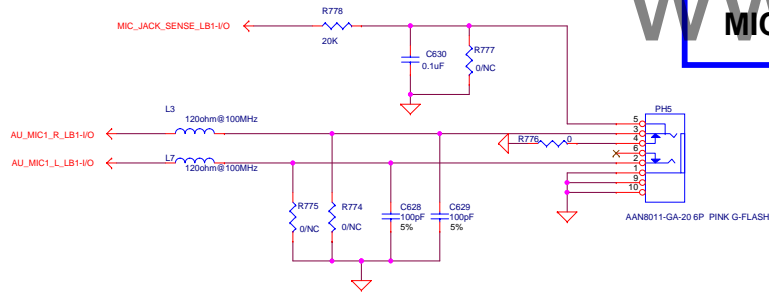


PACKAGE  
ZI90-092D0-24R0\_cen  
朝向

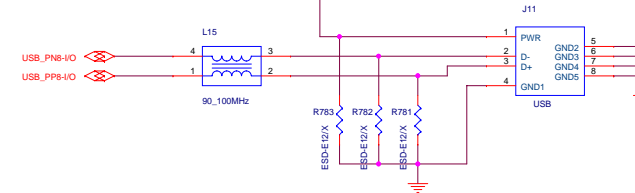


USB PORT

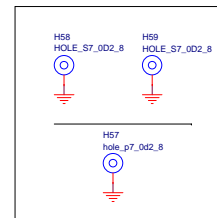
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MIC

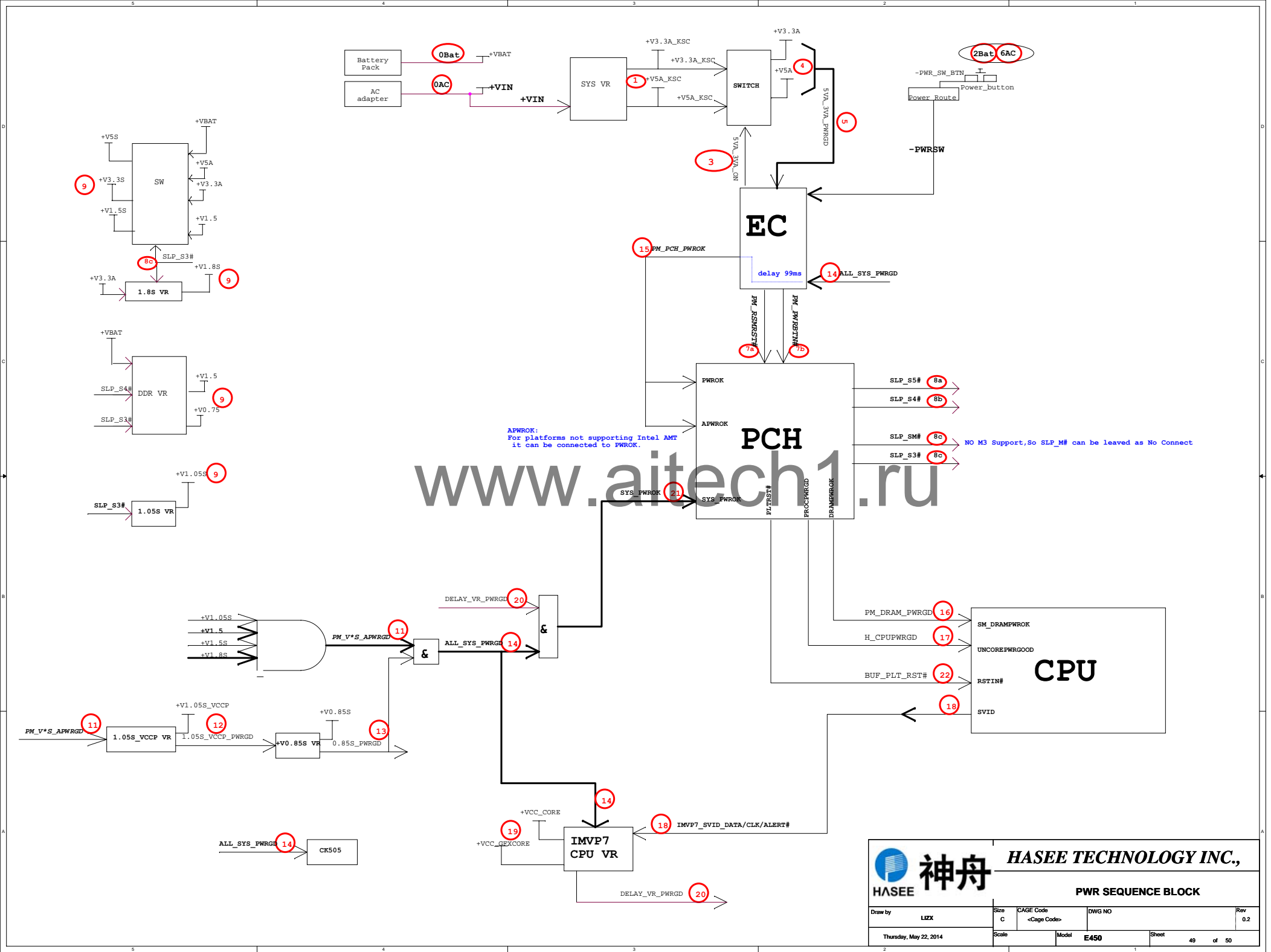


EARPHONE









Change List from Ver01 to Ver02

- 1、Page4,Pull-up R25 from +V3.3S changed to +V3.3A
- 2、Page4, R25,R22,Q65,Q67 all NoStuff  
R23 Stuff
- 3、Page7, PQ45,Q22,R58 all NoStuff  
R59 Stuff
- 4、Page14, U29、R243 、R618、R785、R787、R788、C641 Deleted (SPI1 Flash Del)  
R240、R616、R784 Deleted (SPI0 series-resistor Del)
- 5、Page19,U4,C121,R487 all NOstuff
- 6、Page23,All NoStuff
- 7、Page24,C384,C385,Y5,R522,R600,R718 All NoStuff; R847,C368 Stuff  
同时 Page18, R352 Stuff  
R882 Stuff
- 8、Page28,H33\H32 change the footprint
- 9、Page33, PR152--> 220K,R842-->1M,C537-->0.1UF,C674-->0.01UF(Stuff)
- 10、Page36,C358 change and NC
- 11、Page37, C483 change and NC; R909-->Stuff
- 12、Page14, Isolate HDA SYNC from the codec during the strap:  
Add R787(Stuff),Q51,Q46,R247
- 13、Page44,J17(for bluetooth) pin6, from +V5s changed to +V3.3s
- 14、Layout J6和J14的库要更改及PCH上方邮票孔位置更改
- 15、About the Power:  
L13(2.2u)-->1u-----+V1.5  
C537(0.01U)-->0.1U-----+V5A  
C178-->33nF,R167-->2.87K,R127-->1.2K all 1%-----+VCORE  
C364-->82nF,C367-->2200pF,R177-->665,R144-->2.43K,  
R150-->220K,R172-->270,C286-->560pF,C288-->1nF,C264-->47pF-----+VGFORCE
- 16、Page34, add C641-->0.22uF,C645-->1uF  
change C647 -->33nF
- 17、Page41,add R220 and amplifier for Mic in


Change List from Ver02 to Ver03

- 1、Page35,add R670  
Page36,add FJP33  
(Vccp substitute for V1.05s)
- 2、Page41,con4 change  
add R725

Change List from Ver03 to Ver10

- 1、Page14,add R268\R269
- 2、Page37,add C493

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 神舟		<b>HASEE TECHNOLOGY INC.,</b>			
		<b>PWR SEQUENCE BLOCK</b>			
Draw by	LIZX	Size B	CAGE Code <Cage Code>	DWG NO	Rev 0.2
Thursday, May 22, 2014		Scale	Model <b>E450</b>	Sheet 50 of 50	